

# LM96511

*LM96511 Ultrasound Receive Analog Front End (AFE)*



Literature Number: SNAS476F

# LM96511

## Ultrasound Receive Analog Front End (AFE)

### General Description

The LM96511 is an 8-channel integrated analog front end (AFE) module for multi-channel applications, particularly medical ultrasound. Each of the 8 signal paths consists of a low noise amplifier (LNA), a digitally programmable variable gain amplifier (DVGA) and a 12-bit, 40 to 50 Mega Samples Per Second (MSPS) analog-to-digital converter (ADC) with Instant Overload Recovery (IOR). The architecture of the DVGA is a digitally-controlled linear-in-dB step attenuator driving a fixed-gain post-amplifier (PA). The ADC uses a Continuous-Time-Sigma-Delta ( $\Sigma\Delta$ ) architecture with digital decimation filtering to maximize dynamic performance and provide an alias free input bandwidth to  $ADC\ CLK / 2$ . The ADC digital outputs are serialized and provided on differential LVDS outputs. The ADC includes an on-chip clock cleaner PLL.

In addition, for baseband CW Doppler Beamformer applications, an 8-channel demodulator with 16 discrete phase rotation angles is included.

Selective power reduction is included to minimize consumption of idle sections during interleaved imaging modes.

An SPI™ compatible serial interface allows dynamic digital programming and control. National Semiconductor offers a full development package for sale which includes acquisition analysis hardware and software with user friendly GUI for device programming and control.

### Features

- 8-channel LNA, DVGA, and 12-bit Continuous Time  $\Sigma\Delta$  ADC
- Programmable Active Termination LNA
- 8-channel, integrated CW Doppler Beamformer
- Low-power consumption
- Embedded ADC Digital Filter
- ADC Instant Overload Recovery
- Embedded ADC "clock-cleaning" PLL
- 11 mm x 17 mm RoHS BGA Package

### Key Specifications

(Full path unless noted)

#### B-Mode:

|                                          |                    |
|------------------------------------------|--------------------|
| Total Input Voltage Noise (RTI)          | 0.9 nV/vHz         |
| Max AFE Gain                             | 58 dB              |
| Single-Ended Input Swing                 | 500mVpp            |
| Programmable Maximum DVGA Attenuation    | 38, 36, 34, 32 dB  |
| Programmable Post Amp Gain               | 31 or 38 dB        |
| Attenuator Step Resolution               | 0.05 or 0.1 dB     |
| ADC Resolution                           | 12 bits            |
| Conversion Rate (ADC CLK)                | 40 to 50 MSPS      |
| ADC Digital Filter stop band attenuation | 72 dB              |
| ADC Digital Filter Passband Ripple       | ± 0.01 dB          |
| ADC Instant Overload Recovery            | 1 ADC Clock Period |
| Power Consumption (per channel)          | 110 mW             |

#### CW Doppler Mode:

|                                          |              |
|------------------------------------------|--------------|
| Phase Rotation Resolution                | 22.5 degrees |
| Phase Noise (Per Channel, Offset = 5KHz) | -144 dBc/Hz  |
| Dynamic Range                            | -161 dB/Hz   |
| Amplitude Quadrature Error (I to Q)      | ± 0.04 dB    |
| Phase Quadrature Error (I to Q)          | ± 0.10°      |
| Power Consumption (Per Channel)          | 208 mW       |

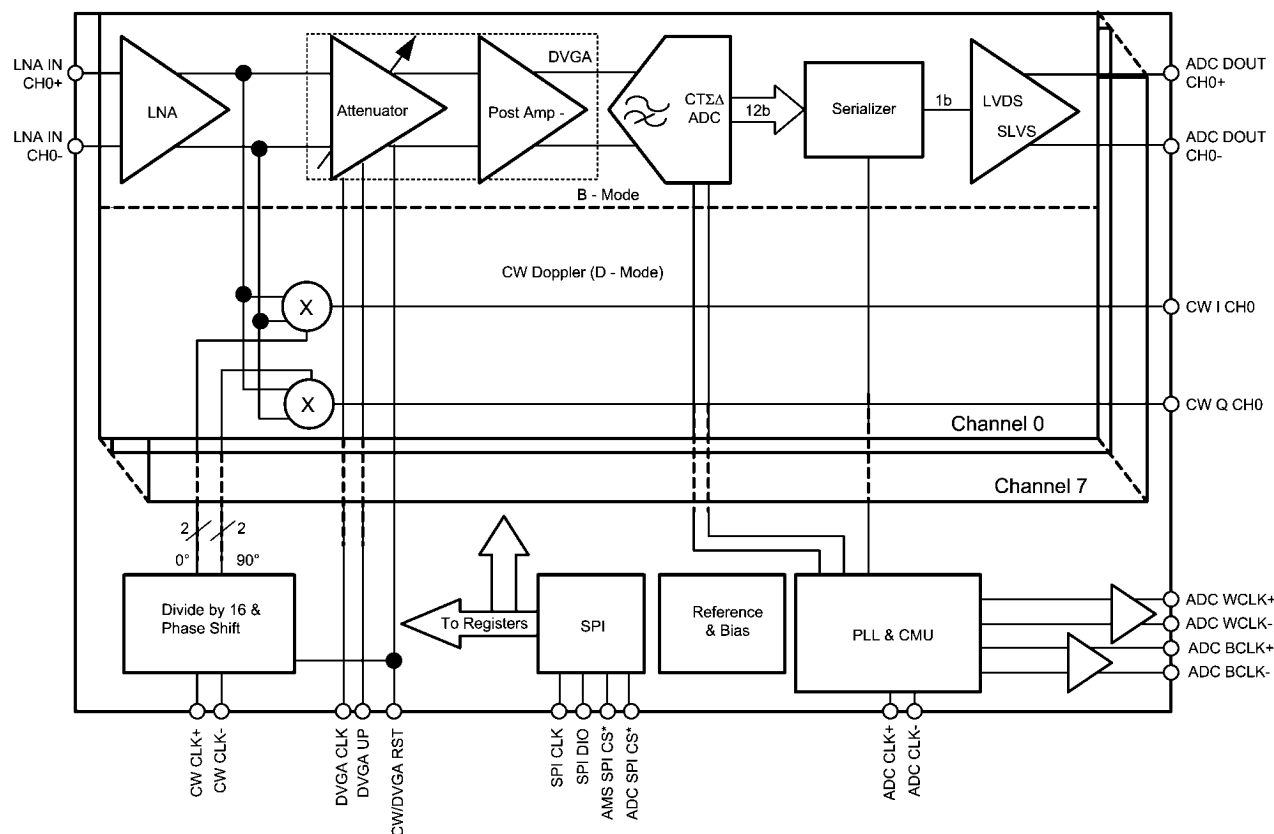
#### Common Specifications:

|                         |             |
|-------------------------|-------------|
| LNA Input Voltage Noise | 0.82 nV/vHz |
| Operating temp. Range   | 0 to +70°C  |

### Applications

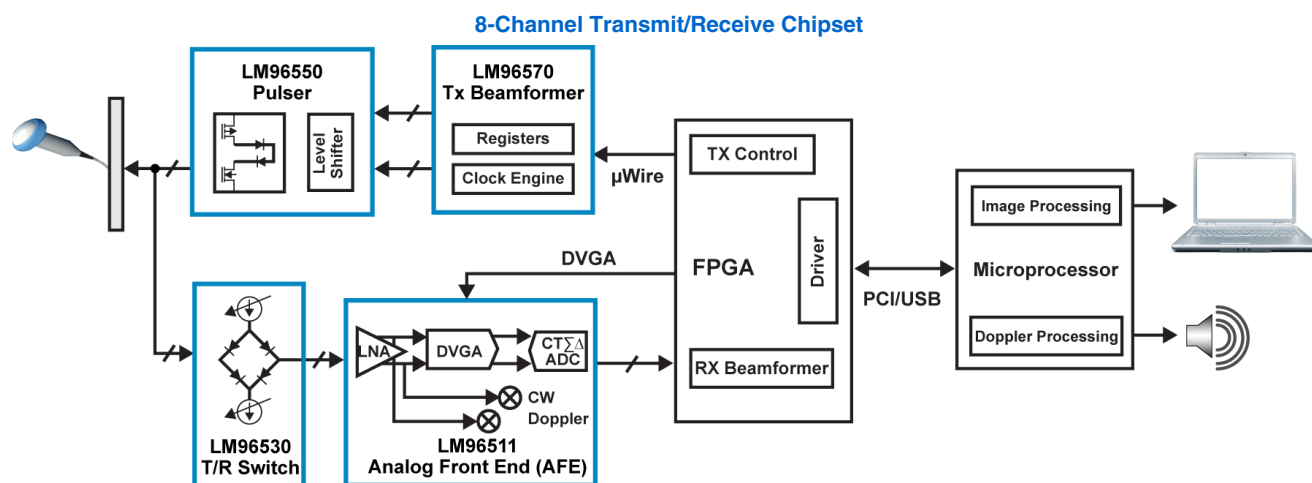
- Ultrasound Imaging
- Communications
- Portable Instrumentation
- Sonar

## Simplified LM96511 Block Diagram



### FIGURE 1. Simplified LM96511 Block Diagram

## Typical Application



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# Connection Diagrams

|   | 1            | 2            | 3          | 4            | 5             | 6             | 7            | 8            | 9            | 10           | 11           | 12      | 13         | 14          | 15           | 16           |   |
|---|--------------|--------------|------------|--------------|---------------|---------------|--------------|--------------|--------------|--------------|--------------|---------|------------|-------------|--------------|--------------|---|
| A | LNA PD       | DVGA PD      | AMP RST    | AMP SPI CS   | ADC SPI CS    | DVGA INIT MSB | AMP DVDD     | AMP DGND     | AGND         | AMP AVCC A   | CW I CH7     | AGND    | AGND       | CW DGND     | CW DGND      | AGND         | A |
| B | DVGA PA HI   | CW AVCC      | SPI CLK    | SPI DIO      | DVGA INIT LSB | AMP IO DVDD   | AMP DVDD     | AMP AVCC A   | DVGA BYP CH7 | CW AVCC      | CW Q CH7     | CW DGND | CW DGND    | CW AVCC     | CW AVCC      | CW I CH6     | B |
| C | NC           | CW AVCC      | AGND       | NC           |               |               |              |              |              |              |              |         |            | CW AVCC     | DVGA BYP CH6 | AMP AVCC A   | C |
| D | LNA IN CH7-  | LNA IN CH7+  | AGND       | LNA OUT CH7- |               |               |              |              |              |              |              |         |            | AMP AVCC A  | AMP AVCC A   | DVGA BYP CH5 | D |
| E | LNA IN CH6+  | CW AVCC      | NC         | AMP AVCC A   |               |               |              |              |              |              |              |         |            | AMP AVCC A  | CW I CH5     | CW AVCC      | E |
| F | LNA OUT CH6- | LNA IN CH6-  | AGND       | CW AVCC      |               |               | AMP THRM GND | AMP THRM GND | AMP THRM GND | AMP THRM GND | AMP THRM GND |         |            | CW Q CH5    | CW DGND      | CW DGND      | F |
| G | LNA IN CH5+  | NC           | AMP AVCC A | CW AVCC      |               |               | AMP THRM GND | AMP THRM GND | AMP THRM GND | AMP THRM GND | AMP THRM GND |         |            | CW Q CH4    | CW AVCC      | CW I CH4     | G |
| H | LNA OUT CH5- | LNA IN CH5-  | AGND       | CW AVCC      |               |               | AMP THRM GND | AMP THRM GND | AMP THRM GND | AMP THRM GND | AMP THRM GND |         |            | AMP DGND    | CW AVCC      | AMP DVDD     | H |
| J | LNA IN CH4+  | NC           | AMP AVCC A | CW AVCC      |               |               | AMP THRM GND | AMP THRM GND | AMP THRM GND | AMP THRM GND | AMP THRM GND |         |            | CW CLK+     | CW CLK-      | AMP AVCC A   | J |
| K | LNA OUT CH4- | LNA IN CH4-  | AGND       | CW AVCC      |               |               | AMP THRM GND | AMP THRM GND | AMP THRM GND | AMP THRM GND | AMP THRM GND |         |            | DVGA CLK    | CW/DVGA RST  | AMP CWDVGA   | K |
| L | LNA IN CH3+  | NC           | AMP AVCC A | CW AVCC      |               |               | AMP THRM GND | AMP THRM GND | AMP THRM GND | AMP THRM GND | AMP THRM GND |         |            | AMP IO DVDD | DVGA BYP CH3 | AMP AVCC A   | L |
| M | LNA OUT CH3- | LNA IN CH3-  | AGND       | AMP AVCC A   |               |               | AMP THRM GND | AMP THRM GND | AMP THRM GND | AMP THRM GND | AMP THRM GND |         |            | CW AVCC     | CW AVCC      | CW I CH3     | M |
| N | LNA IN CH2+  | CW AVCC      | NC         | AMP AVCC A   |               |               | AMP THRM GND | AMP THRM GND | AMP THRM GND | AMP THRM GND | AMP THRM GND |         |            | CW Q CH3    | CW DGND      | CW DGND      | N |
| P | LNA OUT CH2- | LNA IN CH2-  | AGND       | CW AVCC      |               |               |              |              |              |              |              |         |            | AGND        | CW I CH2     | CW AVCC      | P |
| R | LNA IN CH1+  | NC           | AMP AVCC A | AGND         |               |               |              |              |              |              |              |         |            | AMP AVCC A  | AMP AVCC A   | DVGA BYP CH2 | R |
| T | LNA OUT CH1- | LNA IN CH1-  | CW AVCC    | AMP AVCC A   |               |               |              |              |              |              |              |         |            | AMP AVCC A  | AMP AVCC A   | CW AVCC      | T |
| U | LNA IN CH0+  | NC           | AGND       | AMP AVCC A   | AMP DGND      | AGND          | AMP AVCC A   | AMP AVCC A   | CW AVCC      | CW Q CH0     | CW DGND      | AGND    | AMP AVCC A | AMP DVDD    | AMP DVDD     | CW AVCC      | U |
| V | LNA IN CH0-  | LNA OUT CH0- | AGND       | AMP AVCC A   | AMP DVDD      | AMP AVCC A    | NC           | DVGA BYP CH0 | CW AVCC      | CW I CH0     | AGND         | AGND    | AMP AVCC A | CW I CH1    | AGND         | CW DGND      | V |
|   | 1            | 2            | 3          | 4            | 5             | 6             | 7            | 8            | 9            | 10           | 11           | 12      | 13         | 14          | 15           | 16           |   |

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|   | 17           | 18       | 19       | 20   | 21           | 22       | 23           | 24           | 25           | 26           | 27           | 28          | 29          | 30          | 31            | 32            |   |
|---|--------------|----------|----------|------|--------------|----------|--------------|--------------|--------------|--------------|--------------|-------------|-------------|-------------|---------------|---------------|---|
| A | CW Q CH5     | NC       | ADC AVDD | NC   | NC           | ADC CLK- | AGND         | AGND         | AGND         | ADC DVDD     | ADC IO DGND  | ADC IO DGND | ADC WCLK-   | ADC WCLK+   | ADC BCLK-     | ADC BCLK+     | A |
| B | AGND         | NC       | AGND     | AGND | AGND         | ADC CLK+ | AGND         | AGND         | ADC DVDD     | ADC DVDD     | ADC IO DGND  | ADC IO DGND | AGND        | ADC IO DVDD | AGND          | ADC DOUT CH7- | B |
| C | AMP AVCC A   | ADC AVDD | AGND     |      |              |          |              |              |              |              |              |             |             |             | AGND          | ADC DOUT CH7+ | C |
| D | AMP AVCC A   | AGND     | AGND     |      |              |          |              |              |              |              |              |             |             |             | ADC IO DGND   | ADC DOUT CH6- | D |
| E | CW AVCC      | NC       | NC       |      |              |          |              |              |              |              |              |             |             |             | ADC IO DGND   | ADC DOUT CH6+ | E |
| F | AGND         | ADC AVDD | AGND     |      |              |          | ADC THRM GND | ADC THRM GND | ADC THRM GND | ADC THRM GND | ADC THRM GND |             |             |             | AGND          | ADC DOUT CH5- | F |
| G | AGND         | AGND     | AGND     |      |              |          | ADC THRM GND | ADC THRM GND | ADC THRM GND | ADC THRM GND | ADC THRM GND |             |             |             | ADC IO DVDD   | ADC DOUT CH5+ | G |
| H | AMP DVDD     | NC       | NC       |      |              |          | ADC THRM GND | ADC THRM GND | ADC THRM GND | ADC THRM GND | ADC THRM GND |             |             |             | ADC IO DVDD   | ADC DOUT CH4- | H |
| J | DVGA BYP CH4 | ADC AVDD | AGND     |      |              |          | ADC THRM GND | ADC THRM GND | ADC THRM GND | ADC THRM GND | ADC THRM GND |             |             |             | AGND          | ADC DOUT CH4+ | J |
| K | AMP AVCC A   | NC       | AGND     |      |              |          | ADC THRM GND | ADC THRM GND | ADC THRM GND | ADC THRM GND | ADC THRM GND |             |             |             | AGND          | ADC DOUT CH3- | K |
| L | DVGA UP      | AGND     | NC       |      |              |          | ADC THRM GND | ADC THRM GND | ADC THRM GND | ADC THRM GND | ADC THRM GND |             |             |             | AGND          | ADC DOUT CH3+ | L |
| M | AGND         | AGND     | ADC AVDD |      |              |          | ADC THRM GND | ADC THRM GND | ADC THRM GND | ADC THRM GND | ADC THRM GND |             |             |             | ADC IO DGND   | AGND          | M |
| N | AGND         | AGND     | NC       |      |              |          | ADC THRM GND | ADC THRM GND | ADC THRM GND | ADC THRM GND | ADC THRM GND |             |             |             | ADC IO DGND   | ADC DOUT CH2- | N |
| P | CW Q CH2     | AGND     | NC       |      |              |          |              |              |              |              |              |             |             |             | AGND          | ADC DOUT CH2+ | P |
| R | CW AVCC      | AGND     | ADC AVDD |      |              |          |              |              |              |              |              |             |             |             | AGND          | NC            | R |
| T | DVGA BYP CH1 | AGND     | AGND     |      |              |          |              |              |              |              |              |             |             |             | NC            | ADC DOUT CH1- | T |
| U | AMP DGND     | NC       | ADC AVDD | NC   | AGND         | AGND     | ADC RREF     | ADC AVDD     | ADC RST      | ADC AVDD     | ADC DVDD     | ADC AVDD    | ADC IO DGND | AGND        | ADC IO DVDD   | ADC DOUT CH1+ | U |
| V | CW Q CH1     | NC       | AGND     | NC   | ADC VREF GND | ADC VREF | ADC LPF BYP  | AGND         | AGND         | ADC CWDVGA   | ADC AVDD     | ADC DVDD    | ADC AVDD    | ADC IO DGND | ADC DOUT CH0+ | ADC DOUT CH0- | V |
|   | 17           | 18       | 19       | 20   | 21           | 22       | 23           | 24           | 25           | 26           | 27           | 28          | 29          | 30          | 31            | 32            |   |

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FIGURE 2. 376-Pin BGA Package Top View (18 Rows by 32 Columns)

## Ordering Information

| Order Number     | Package Type | NSC Package Drawing | Supplied As |
|------------------|--------------|---------------------|-------------|
| LM96511CCSM NOPB | TFBGA 376    | SLM376A             | Trays       |

SPI™ is a trademark of Motorola Inc.

TRI\_STATE® is a registered trademark of National Semiconductor Corporation.

## Pin Descriptions

| Ball Id.<br>(Row_Column) | Pin Name      | Function | Description                           |
|--------------------------|---------------|----------|---------------------------------------|
| <b>Amplifier Signals</b> |               |          |                                       |
| U1                       | LNA IN CH0+   | Input    | LNA Non-Inverting Input               |
| R1                       | LNA IN CH1+   |          |                                       |
| N1                       | LNA IN CH2+   |          |                                       |
| L1                       | LNA IN CH3+   |          |                                       |
| J1                       | LNA IN CH4+   |          |                                       |
| G1                       | LNA IN CH5+   |          |                                       |
| E1                       | LNA IN CH6+   |          |                                       |
| D2                       | LNA IN CH7+   |          |                                       |
| V1                       | LNA IN CH0-   |          | LNA Inverting Input                   |
| T2                       | LNA IN CH1-   |          |                                       |
| P2                       | LNA IN CH2-   |          |                                       |
| M2                       | LNA IN CH3-   |          |                                       |
| K2                       | LNA IN CH4-   |          |                                       |
| H2                       | LNA IN CH5-   |          |                                       |
| F2                       | LNA IN CH6-   |          |                                       |
| D1                       | LNA IN CH7-   |          |                                       |
| V2                       | LNA OUT CH0-  | Output   | LNA Inverting Output                  |
| T1                       | LNA OUT CH1-  |          |                                       |
| P1                       | LNA OUT CH2-  |          |                                       |
| M1                       | LNA OUT CH3-  |          |                                       |
| K1                       | LNA OUT CH4-  |          |                                       |
| H1                       | LNA OUT CH5 - |          |                                       |
| F1                       | LNA OUT CH6-  |          |                                       |
| D4                       | LNA OUT CH7-  |          |                                       |
| V8                       | DVGA BYP CH0  | Bypass   | Decoupling Capacitor to Analog Ground |
| T17                      | DVGA BYP CH1  |          |                                       |
| R16                      | DVGA BYP CH2  |          |                                       |
| L15                      | DVGA BYP CH3  |          |                                       |
| J17                      | DVGA BYP CH4  |          |                                       |
| D16                      | DVGA BYP CH5  |          |                                       |
| C15                      | DVGA BYP CH6  |          |                                       |
| B9                       | DVGA BYP CH7  |          |                                       |
| J14                      | CW CLK+       | Input    | CW DOPPLER Differential Input Clock + |
| J15                      | CW CLK-       |          |                                       |
| V10                      | CW I CH0      | Output   | CW DOPPLER In-Phase output current    |
| V14                      | CW I CH1      |          |                                       |
| P15                      | CW I CH2      |          |                                       |
| M16                      | CW I CH3      |          |                                       |
| G16                      | CW I CH4      |          |                                       |
| E15                      | CW I CH5      |          |                                       |
| B16                      | CW I CH6      |          |                                       |
| A11                      | CW I CH7      |          |                                       |

| Ball Id.<br>(Row_Column) | Pin Name             | Function | Description                                                                                                                                                                                                                                                                                                                                                                                           |
|--------------------------|----------------------|----------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| U10                      | CW Q CH0             | Output   | CW DOPPLER Quadrature-Phase output current                                                                                                                                                                                                                                                                                                                                                            |
| V17                      | CW Q CH1             |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| P17                      | CW Q CH2             |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| N14                      | CW Q CH3             |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| G14                      | CW Q CH4             |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| F14                      | CW Q CH5             |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| A17                      | CW Q CH6             |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| B11                      | CW Q CH7             |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| Amplifier Controls       |                      |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| K14                      | DVGA CLK             | Input    | DVGA GAIN Clock                                                                                                                                                                                                                                                                                                                                                                                       |
| L17                      | DVGA UP              |          | 1 = Increment DVGA gain<br>0 = Decrement DVGA gain                                                                                                                                                                                                                                                                                                                                                    |
| A6                       | DVGA INIT MSB        |          | DVGA Initial Gain Control. Sets the initial DVGA gain. See application section.                                                                                                                                                                                                                                                                                                                       |
| B5                       | DVGA INIT LSB        |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| K15                      | CW/DVGA RST          |          | 1 = CW DOPPLER Phase and DVGA Gain Reset                                                                                                                                                                                                                                                                                                                                                              |
| K16                      | AMP CW/DVGA          |          | 0 = B-mode<br>1 = CW DOPPLER mode                                                                                                                                                                                                                                                                                                                                                                     |
| A1                       | LNA PD               |          | 1 = LNA Power-down                                                                                                                                                                                                                                                                                                                                                                                    |
| A2                       | DVGA PD              |          | 1 = DVGA Power-down                                                                                                                                                                                                                                                                                                                                                                                   |
| A3                       | AMP RST              |          | 1 = Reset all Amplifier SPI™ Registers                                                                                                                                                                                                                                                                                                                                                                |
| B1                       | DVGA PA HI           |          | Post Amplifier Gain:<br>1= 38 dB<br>0= 31 dB                                                                                                                                                                                                                                                                                                                                                          |
| ADC Signals              |                      |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| B22<br>A22               | ADC CLK+<br>ADC CLK- | Input    | Differential Input Clock. The input clock must lie in the range of 40 MHz to 50 MHz. It is used by the PLL to generate the internal sampling clocks .                                                                                                                                                                                                                                                 |
| V31                      | ADC DOUT CH0+        | Output   | Differential Serial Outputs for channels 0 to 7. Each pair of outputs provides the serial output for the specific channel. The default output is LVDS format, but programming the appropriate control registers, the output format can be changed to SLVS .<br>By programming TX_term (bit 4) in the LVDS Control register, it is possible to internally terminate these outputs with 100Ω resistors. |
| U32                      | ADC DOUT CH1+        |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| P32                      | ADC DOUT CH2+        |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| L32                      | ADC DOUT CH3+        |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| J32                      | ADC DOUT CH4+        |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| G32                      | ADC DOUT CH5+        |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| E32                      | ADC DOUT CH6+        |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| C32                      | ADC DOUT CH7+        |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| V32                      | ADC DOUT CH0-        |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| T32                      | ADC DOUT CH1-        |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| N32                      | ADC DOUT CH2-        |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| K32                      | ADC DOUT CH3-        |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| H32                      | ADC DOUT CH4-        |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| F32                      | ADC DOUT CH5-        |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| D32                      | ADC DOUT CH6-        |          |                                                                                                                                                                                                                                                                                                                                                                                                       |
| B32                      | ADC DOUT CH7-        |          |                                                                                                                                                                                                                                                                                                                                                                                                       |

| Ball Id.<br>(Row_Column)  | Pin Name                     | Function     | Description                                                                                                                                                                                                                                                                                                                            |
|---------------------------|------------------------------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| A30<br>A29                | ADC WCLK+<br>ADC WCLK-       | Output       | Word Clock. Differential output frame clock used to indicate the bit boundary of each data sample. Information on timing can be seen in the Electrical Specifications section of the datasheet. By programming TX_term (bit 4) in the LVDS Control register, it is possible to internally terminate these outputs with 100Ω resistors. |
| A32<br>A31                | ADC BCLK+<br>ADC BCLK-       |              | Bit clock. Differential output clock used for sampling the serial outputs. Information on timing can be seen in the Electrical Specifications section of the datasheet. By programming TX_term (bit 4) in the LVDS Control register, it is possible to internally terminate these outputs with 100Ω resistors.                         |
| ADC Controls              |                              |              |                                                                                                                                                                                                                                                                                                                                        |
| U25                       | <div>_____</div> ADC RST     | Input        | This pin is an active low reset for the entire ADC, both analog and digital components. The pin must be held low for 500 ns then returned to high in order to ensure that the chip is reset correctly.                                                                                                                                 |
| V26                       | ADC CW/DVGA                  | Input        | 0 = B-mode<br>1 = CW DOPPLER mode, PLL and References are still active to minimize recovery time.                                                                                                                                                                                                                                      |
| V22                       | ADC VREF                     |              | ADC Optional External Reference Voltage; Improves channel-to-channel and converter-to-converter matching.                                                                                                                                                                                                                              |
| V21                       | ADC VREF GND                 |              | If Internal Reference is used, connect to AGND.                                                                                                                                                                                                                                                                                        |
| U23                       | ADC RREF                     | Output       | External 10k ±1% resistor to ADC Analog GND. Used to set internal bias currents. Required regardless of the type of reference used.                                                                                                                                                                                                    |
| V23                       | ADC LPF BYP                  | Bypass       | Capacitor required by the Modulator DAC's LP Filter. Must be at least 100 nF to ADC Analog GND. Can be increased to 10 μF to minimize close-in phase noise.                                                                                                                                                                            |
| SPI™ Compatible Interface |                              |              |                                                                                                                                                                                                                                                                                                                                        |
| B3                        | SPI™ CLK                     | Input        | SPI™ clock                                                                                                                                                                                                                                                                                                                             |
| B4                        | SPI™ DIO                     | Input/Output | SPI™ Data Input/Output                                                                                                                                                                                                                                                                                                                 |
| A5                        | <div>_____</div> ADC SPI™ CS | Input        | 0 = ADC SPI™ Chip Select                                                                                                                                                                                                                                                                                                               |
| A4                        | <div>_____</div> AMP SPI™ CS |              | 0 = Amplifier SPI™ Chip Select.                                                                                                                                                                                                                                                                                                        |

| Ball Id.<br>(Row_Column)                                                                                                                                 | Pin Name    | Function | Description                                                          |
|----------------------------------------------------------------------------------------------------------------------------------------------------------|-------------|----------|----------------------------------------------------------------------|
| <b>Power and Ground</b>                                                                                                                                  |             |          |                                                                      |
| A10, B8, C16, C17,<br>D14, D15, D17, E4,<br>E14, G3, J3, J16, K17,<br>L3, L16, M4, N4, R3,<br>R14, R15, T4, T14,<br>T15, U4, U7, U8, U13,<br>V4, V6, V13 | AMP AVCC A  | Power    | Amplifier Analog Power<br>Nominally +3.3V.                           |
| B10, B14, B15, C14,<br>E16, E17, H15, G15,<br>M14, M15, P16, R17,<br>T16, U9, U16, V9, B2,<br>C2, E2, F4, G4, H4,<br>J4, K4, L4, N2, P4, T3              | CW AVCC     |          | CW DOPPLER Analog Power<br>Nominally +5.0V.                          |
| V5, A7, B7, H16, H17,<br>U14, U15                                                                                                                        | AMP DVDD    |          | DVGA Digital Power. Nominally +3.3V.                                 |
| B6, L14                                                                                                                                                  | AMP IO DVDD |          | Amplifier IO Digital Power. Connect to ADC IO DVDD. Nominally +1.2V. |
| B30, G31, H31, U31                                                                                                                                       | ADC IO DVDD |          | ADC IO Digital Power. Nominally +1.2V.                               |
| A19, C18, F18, J18,<br>M19, R19, U19, U24,<br>U26, U28, V27, V29                                                                                         | ADC AVDD    |          | ADC Analog Power. Nominally +1.2V.                                   |
| A26, B25, B26, U27,<br>V28                                                                                                                               | ADC DVDD    |          | ADC Digital Power. Nominally +1.2V .                                 |

| Ball Id.<br>(Row_Column)                                                                                                                                                                                                                                                                                           | Pin Name     | Function | Description                      |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------|----------|----------------------------------|
| A9, A12, A13, A16, A23, A24, A25, B17, B19, B20, B21, B23, B24, B29, B31, C3, C19, C31, D3, D18, D19, F3, F17, F19, F31, G17, G18, G19, H3, J19, J31, K3, K19, K31, L18, L31, M3, M17, M18, M32, N17, N18, P3, P14, P18, P31, R4, R18, R31, T18, T19, U3, U6, U12, U21, U22, U30, V3, V11, V12, V15, V19, V24, V25 | AGND         | Ground   | Analog Ground                    |
| F7, F8, F9, F10, F11, G7, G8, G9, G10, G11, H7, H8, H9, H10, H11, J7, J8, J9, J10, J11, K7, K8, K9, K10, K11, L7, L8, L9, L10, L11, M7, M8, M9, M10, M11, N7, N8, N9, N10, N11                                                                                                                                     | AMP THRM GND |          | Thermal Ground (Connect to AGND) |
| F23, F24, F25, F26, F27, G23, G24, G25, G26, G27, H23, H24, H25, H26, H27, J23, J24, J25, J26, J27, K23, K24, K25, K26, K27, L23, L24, L25, L26, L27. M23, M24, M25, M26, M27, N23, N24, N25, N26, N27                                                                                                             | ADC THRM GND |          |                                  |
| A14, A15, B12, B13, F15, F16, N15, N16, U11, V16                                                                                                                                                                                                                                                                   | CW DGND      |          | Digital Ground                   |
| A8, H14, U5, U17                                                                                                                                                                                                                                                                                                   | AMP DGND     |          |                                  |
| A27, A28, B27, B28, D31, E31, M31, N31, U29, V30                                                                                                                                                                                                                                                                   | ADC IO DGND  |          |                                  |
| No Connect                                                                                                                                                                                                                                                                                                         |              |          |                                  |
| Important: "NC" pins should be left unconnected. Any connection to these pins could affect performance and functionality.                                                                                                                                                                                          |              |          |                                  |
| A18, A20, A21, B18, C1, E3, E18, E19, G2, H18, H19, J2, K18, L2, L19, N3, N19, P19, R2, U2, U18, U20, V18, V20, R32, T31, V7, C4                                                                                                                                                                                   | NC           |          | Do Not Connect                   |

## Absolute Maximum Ratings *(Note 1)*

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

|                                                                                  |                  |
|----------------------------------------------------------------------------------|------------------|
| Storage Temperature Range                                                        | TBD              |
| Supply Voltage (CW AVCC)                                                         | -0.3V and +6V    |
| Supply Voltage (AMP AVCC A, AMP DVDD)                                            | -0.3V and +3.63V |
| Supply Voltage (ADC AVDD, ADC DVDD)                                              | -0.3V and +1.44V |
| IO Supply Voltage (AMP IO DVDD, ADC IO DVDD)                                     | -0.3V and +2.0V  |
| Voltage at Analog Inputs                                                         | -0.3V and +2.0V  |
| Voltage at SPI™ Compatible inputs (SPI™ CLK, SPI™ DIO, AMP SPI™ CS, ADC SPI™ CS) | -0.3V and +2.0V  |
| Input Current at any pin other than a Supply Voltage and LNA Inputs              | 25 mA            |
| LNA Inputs                                                                       | 2.6 Vpp & ±10 mA |

|                                                                       |                  |
|-----------------------------------------------------------------------|------------------|
| Supply Voltage (AMP AVCC A, AMP DVDD)                                 | +3.13V to 3.47V  |
| Supply Voltage (ADC AVDD, ADC DVDD)                                   | +1.14V to +1.26V |
| IO Supply Voltage (AMP IO DVDD, ADC io DVD)                           | +1.14V to +1.89V |
| Analog Inputs                                                         | TBD              |
| SPI™ Compatible Inputs (SPI™ CLK, SPI™ DIO, AMP SPI™ CS, ADC SPI™ CS) | +1.14V to +1.89V |
| ADC CLK Input Frequency                                               | 40 to 50 MHz     |
| ADC CLK Duty Cycle                                                    | 30 to 70%        |
| DVGA CLK Frequency                                                    | < 100 MHz        |
| Ground Difference IAGND - DGNDI                                       | 50 mV            |
| ESD Tolerance( <i>Note 19</i> ):                                      |                  |
| Human Body Model                                                      | 1500V            |
| Machine Model                                                         | 100V             |
| Charge Device Model                                                   | 750V             |

## Operating Ratings

(*Note 1*)

|                             |                  |
|-----------------------------|------------------|
| Operation Temperature Range | 0°C to +70°C     |
| Supply Voltage (CW AVCC)    | +4.75V to +5.25V |

## AFE Electrical Characteristics (B-Mode)

Unless otherwise noted, specified limits apply for AMP AVCC A = **3.3V**, CW AVCC = **5V**, AMP IO DVDD = ADC IO DVDD = **1.2V**, ADC AVDD = ADC DVDD = **1.2V**, Full Scale ADC Output with RF Input at 5 MHz, DVGA PA HI = LO; AMP CW/DVGA pin = ADC CW/DVGA pin = LO,  $F_{CLK} = 40$  MSPS; Clock duty cycle stabilization enabled; IOR On Mode. All 8 channels powered. **Boldface limits** apply for  $T_A = T_{MIN}$  to  $T_{MAX}$ ; All other limits apply for  $T_A = +25^\circ\text{C}$ .

| Parameter                                                | Conditions                                                                   | Min | Typ          | Max   | Units            |
|----------------------------------------------------------|------------------------------------------------------------------------------|-----|--------------|-------|------------------|
| Total Input (RTI) Voltage Noise                          | See , No Active Feedback, Input AC shorted to ground                         |     | 0.9          |       | nV/√Hz           |
| Noise Figure                                             | Equivalent 50Ω termination using Active Feedback ( $R_{FB} = 301\Omega$ )    |     | 3.7          |       | dB               |
| Single-Ended LNA Input Swing                             | 1 dB SNR Loss (TGC in Operation). See ( <i>Note 2</i> ) & ( <i>Note 22</i> ) |     | 380          |       | mV <sub>pp</sub> |
| Externally Programmable Input Resistance Range (overall) |                                                                              | 50  |              | 2k    | Ω                |
| Offset Related Full Scale Amplitude Loss                 | Max DVGA Gain. 1δ, See ( <i>Note 18</i> )                                    |     | -0.23        |       | dB               |
|                                                          | Max DVGA Gain, IOR Off Mode. 1δ, See ( <i>Note 18</i> )                      |     | -0.15        |       |                  |
| Offset Tempco                                            |                                                                              |     | -0.22        |       | LSB/°C           |
| Overload Recovery                                        | Max DVGA Gain, Error < ±1%                                                   |     | 1/ $f_{CLK}$ |       | seconds          |
|                                                          | Max DVGA Gain, Error < ±1%                                                   |     | 1/ $f_{CLK}$ |       | seconds          |
| Ch-Ch Gain Match                                         | Worst case across DVGA Gain Range                                            |     | ±0.06        | ±0.2  | dB               |
| Ch-Ch Phase Match                                        | Worst case across DVGA Gain Range                                            |     | ±0.35        | ±0.75 | °C               |
| Ch-Ch Group Delay Match                                  |                                                                              |     | ±0.20        | ±0.80 | ns               |
| Ch-Ch Crosstalk                                          | Min DVGA Gain. See ( <i>Note 9</i> )                                         |     | -61          |       | dBc              |
|                                                          | Min DVGA Gain. See ( <i>Note 9</i> )                                         |     | -62          |       |                  |
|                                                          | Min DVGA Gain. See ( <i>Note 9</i> )                                         |     | -62          |       |                  |
| Bandwidth                                                | -3 dB, Small Signal                                                          |     | $f_{CLK}/2$  |       | MHz              |

| Parameter                                                                 | Conditions                                                                                              | Min | Typ | Max        | Units         |
|---------------------------------------------------------------------------|---------------------------------------------------------------------------------------------------------|-----|-----|------------|---------------|
| SNR                                                                       | Mid DVGA gain, -6dB FS, DVGA PA HI pin= LO                                                              | 60  | 63  |            | dBFS          |
|                                                                           | Mid DVGA gain, -1dB FS, DVGA PA HI pin= LO                                                              |     | 62  |            |               |
|                                                                           | Mid DVGA gain, -6dB FS, DVGA PA HI pin= HI                                                              |     | 57  |            |               |
|                                                                           | Mid DVGA gain, -1dB FS, DVGA PA HI pin= HI                                                              |     | 56  |            |               |
| HD2                                                                       | $f_{in} = 5 \text{ MHz}$ , -6dBFS, Mid DVGA Gain                                                        |     | -72 | -60        | dBFS          |
|                                                                           | $f_{in} = 5 \text{ MHz}$ , -1dBFS, Mid DVGA Gain                                                        |     | -68 |            |               |
| HD3                                                                       | $f_{in} = 5 \text{ MHz}$ , -6dBFS, Mid DVGA Gain                                                        |     | -52 |            | dBFS          |
|                                                                           | $f_{in} = 5 \text{ MHz}$ , -1dBFS, Mid DVGA Gain                                                        |     | -43 |            |               |
| DVGA Clock Feedthrough                                                    | DVGA CLK frequency = 7.5MHz                                                                             |     | -95 |            | dBFS          |
| AM Sidebands                                                              | Half Step Disabled                                                                                      |     | TBD |            | dBFS          |
|                                                                           | Half Step Enabled                                                                                       |     | TBD |            |               |
| Spurious Noise near $f_{in}$ , $f_{in} \pm (3/8 \times f_{in})$           | $f_{in} = 2 \text{ to } 20 \text{ MHz}$                                                                 |     | -84 |            | dBFS          |
| Spurious Noise near $2f_{in}$ , $2 \times f_{in} \pm (3/4 \times f_{in})$ |                                                                                                         |     | -83 |            | dBFS          |
| SFDR                                                                      | $f_{in} = 5 \text{ MHz}$ , -6 dBFS, Mid DVGA Gain                                                       |     | 88  |            | dBFS          |
|                                                                           | $f_{in} = 5 \text{ MHz}$ , -1 dBFS, Mid DVGA Gain                                                       |     | 82  |            |               |
| Power Consumption                                                         | Active Mode, IO DVDD = 1.2V                                                                             |     | 880 | <b>910</b> | mW            |
|                                                                           | Active Mode, IO DVDD = 1.8V                                                                             |     | 905 |            |               |
|                                                                           | Power Down                                                                                              |     | 50  |            |               |
| Power Supply Current                                                      | AMP AVCC = 3.3V                                                                                         |     | 155 |            | mA            |
|                                                                           | AMP DVDD = 3.3V                                                                                         |     | 1.6 |            |               |
|                                                                           | CW AVCC = 5.0V                                                                                          |     | 3.2 |            |               |
|                                                                           | ADC AVDD = 1.2V                                                                                         |     | 147 |            |               |
|                                                                           | ADC DVDD = 1.2V                                                                                         |     | 104 |            |               |
|                                                                           | IO DVDD = 1.2V                                                                                          |     | 35  |            |               |
| Wake-up Time                                                              | From Stand-By (From CW DOPPLER to B Mode when AMP CW/DVGA pin is switched from HI to LO). See (Note 17) |     | 15  | 20         | $\mu\text{s}$ |

## CW Doppler Electrical Characteristics

Unless otherwise noted, specified limits apply for AMP AVCC A = **3.3V**, CW AVCC = **5V**, AMP IO DVDD = ADC IO DVDD = **1.2V**, ADC AVDD = ADC DVDD = **1.2V**; Full Scale ADC Output with RF Input at 5 MHz; CW CLK = 80 MHz (LVPECL levels), AMP CW/DVGA pin = ADC CW/DVGA = HI. **Boldface limits** apply for  $T_A = T_{MIN}$  to  $T_{MAX}$ ; All other limits apply for  $T_A = +25^\circ\text{C}$ .

| Parameter                         | Conditions                                                                                              | Min       | Typ        | Max         | Units                  |
|-----------------------------------|---------------------------------------------------------------------------------------------------------|-----------|------------|-------------|------------------------|
| Phase Noise                       | $f_{\text{OFFSET}} = 5\text{kHz}$ with LNA Input = 240 mV <sub>PP</sub> @ 5 MHz. See (Note 6)           |           | -144       |             | dBc/Hz                 |
| Dynamic Range (DNR)               | IP1dB referred to RTI Noise                                                                             |           | -161       |             | dB/Hz                  |
| RTI Noise                         |                                                                                                         |           | 1.2        |             | nV/ $\sqrt{\text{Hz}}$ |
| Single-Ended LNA Input Swing      | 1dB Compression (CW Doppler Mode). (IP1dB). See (Note 2) & (Note 22)                                    |           | 500        |             | mV <sub>PP</sub>       |
| Phase Rotation Resolution         | 16 dynamically selectable angles                                                                        |           | 22.5       |             | degrees                |
| Phase Temperature Coefficient     | I or Q. See (Note 7)                                                                                    |           | $\pm 20$   |             | milli°C                |
| Phase Quadrature Accuracy         | I to Q. $\pm 6^\circ$ . See (Note 7) & (Note 12)                                                        |           | $\pm 0.10$ |             | °C                     |
| Phase Match                       | I to I or Q to Q. See (Note 8) & (Note 12)                                                              |           | $\pm 0.35$ |             | °C                     |
| Amplitude Match                   | I to Q. See (Note 8) & (Note 12)                                                                        |           | $\pm 0.04$ |             | dB                     |
| Amplitude Temperature Coefficient | I or Q. See (Note 7)                                                                                    |           | $\pm 11$   |             | mdB/°C                 |
| CW CLK Input Freq Range           | See (Note 11)                                                                                           | 12        |            | 240         | MHz                    |
| RF Input Freq Range               | CW CLK = 16 x RF Input frequency. See (Note 11)                                                         | 0.7       |            | 15          | MHz                    |
| Third order IMD (IMD3)            | Equal tones (f1 = 10 KHz offset, f2 = 15 KHz offset). See (Note 14)                                     |           | -72        |             | dBc                    |
|                                   | Unequal tones. (f1 = 10 KHz offset, f2 = 15 KHz offset). See (Note 14)                                  |           | -50        |             |                        |
| Channel-to-Channel Crosstalk      | "I" or "Q" output of undriven channel relative to driven channel                                        |           | -95        |             | dBc                    |
| Output Signal Current             | I or Q, Per Channel, LNA Input = 380mV <sub>PP</sub>                                                    | $\pm 3.9$ | $\pm 4.2$  | $\pm 4.5$   | mA                     |
| Output Noise Current Density      | $f_{\text{OFFSET}} = 5\text{kHz}$ with no LNA Input                                                     |           | 53         |             | pA/ $\sqrt{\text{Hz}}$ |
| Output Noise Correlation Factor   | Channels 0 - 7 summed together                                                                          |           | TBD        |             | dB                     |
| Output Compliance Range           |                                                                                                         |           | 2.1 to 3.6 |             | V                      |
| Output Impedance                  | DC to 50 kHz                                                                                            |           | 100k       |             | $\Omega$               |
| Power Consumption                 | Active Mode (ADC CW/DVGA pin = HI)                                                                      |           | 1.66       | <b>1.70</b> | W                      |
|                                   | Power Down                                                                                              |           | 0.05       |             |                        |
| Wake-up Time                      | From Stand-By (From CW DOPPLER to B Mode when AMP CW/DVGA pin is switched from HI to LO). See (Note 17) |           | 13         | TBD         | $\mu\text{s}$          |

## LNA Electrical Characteristics

| Parameter                     | Conditions                                                             | Min | Typ  | Max | Units                  |
|-------------------------------|------------------------------------------------------------------------|-----|------|-----|------------------------|
| Input Voltage Noise           | See (Note 2)                                                           |     | 0.82 |     | nV/ $\sqrt{\text{Hz}}$ |
| Input Current Noise           | $R_S=50\Omega$ , $f=1\text{MHz}$ , No Active Termination, See (Note 2) |     | 5    |     | pA/ $\sqrt{\text{Hz}}$ |
| Input Capacitance             | Each Input to ground                                                   |     | 17   |     | pF                     |
| Single-Ended Input Swing      | 1 dB Compression. See (Note 2) & (Note 22)                             |     | 500  |     | mV p-p                 |
| Max Differential Output Swing |                                                                        |     | 3    |     | Vp-p                   |
| HD2                           | $f_{in} = 5\text{MHz}$ , -6dBFS out, Minimum DVGA                      |     | -55  |     | dBc                    |
| HD3                           | Gain                                                                   |     | -52  |     |                        |
| Output VCM                    |                                                                        |     | 1.65 |     | V                      |
| LNA Gain                      | Single-ended In to Differential Out                                    | 19  | 20   | 21  | dB                     |
| Power Consumption             | Total, 8 channels Active                                               |     | 280  |     | mW                     |
| Power Up Time                 | From Power-Down mode                                                   |     | 10   |     | $\mu\text{s}$          |

## DVGA Electrical Characteristics

Unless otherwise noted, specified limits apply for AMP AVCC A = AMP DVDD = **3.3V**; "half-step" enabled (SPI™ Register 1Ah[3] = 1),  $f_{in} = 5\text{MHz}$ . **Boldface** limits apply for  $T_A = T_{MIN}$  to  $T_{MAX}$ ; All other limits apply for  $T_A = +25^\circ\text{C}$ .

| Parameter                                         | Conditions                                                                                   | Min  | Typ  | Max        | Units                  |
|---------------------------------------------------|----------------------------------------------------------------------------------------------|------|------|------------|------------------------|
| Post Amp Gain                                     | DVGA PA HI = HI                                                                              | 36.0 | 38.0 | 40.0       | dB                     |
|                                                   | DVGA PA HI = LO                                                                              | 28.4 | 31   | 32.4       |                        |
| Selectable DVGA Initial Attenuation (See Table 4) | DVGA UP pin = HI<br>CW/DVGA RST pin = HI<br>DVGA INIT MSB pin = LO<br>DVGA INIT LSB pin = LO | 36.0 | 38.0 | 40.0       | dB                     |
|                                                   | DVGA UP pin = HI<br>CW/DVGA RST pin = HI<br>DVGA INIT MSB pin = LO<br>DVGA INIT LSB pin = HI | 34.0 | 36.0 | 38.0       |                        |
|                                                   | DVGA UP pin = HI<br>CW/DVGA RST pin = HI<br>DVGA INIT MSB pin = HI<br>DVGA INIT LSB pin = LO | 32.0 | 34.0 | 36.0       |                        |
|                                                   | DVGA UP pin = HI<br>CW/DVGA RST pin = HI<br>DVGA INIT MSB pin = HI<br>DVGA INIT LSB pin = HI | 30.0 | 32.0 | 34.0       |                        |
|                                                   | DVGA UP pin = LO<br>CW/DVGA RST pin = HI<br>DVGA INIT MSB pin = X<br>DVGA INIT LSB pin = X   | -1.6 | 0    | 2.4        |                        |
|                                                   |                                                                                              |      |      |            |                        |
| Attenuation Steps                                 | SPI™ Register 1Ah[3] = 0                                                                     |      | 0.05 |            | dB                     |
|                                                   | SPI™ Register 1Ah[3] = 1                                                                     |      | 0.1  |            |                        |
| Attenuation error from nominal                    | See (Note 10)                                                                                |      |      | $\pm 0.15$ | dB                     |
| Attenuator step error from 0.05dB                 |                                                                                              |      |      | $\pm 20$   | mdB                    |
| PA Input Noise                                    |                                                                                              |      | 3.6  |            | nV/ $\sqrt{\text{Hz}}$ |
| Power-Up Time                                     | From Power-Down mode                                                                         |      | 0.1  |            | $\mu\text{s}$          |

## ADC Electrical Characteristics

Unless otherwise noted, specified limits apply for ADC AVDD = ADC DVDD = 1.2V, ADC IO DVDD = 1.2V;  $F_{CLK} = 40$  MSPS; Clock duty cycle stabilization enabled; IOR On Mode. AMP CW/DVGA pin = ADC CW/DVGA pin = LO. **Boldface limits** apply for  $T_A = T_{MIN}$  to  $T_{MAX}$ ; All other limits apply for  $T_A = +25^\circ\text{C}$ .

| Parameter                                        | Conditions                                                            | Min | Typ  | Max  | Units              |
|--------------------------------------------------|-----------------------------------------------------------------------|-----|------|------|--------------------|
| Resolution                                       | No missing codes. See (Note 11)                                       |     |      | 12   | bits               |
| Sampling Rate                                    | ADC CLK                                                               | 40  |      | 50   | MSPS               |
| Conversion Latency                               | Equalizer On                                                          | 19  | 19   | 19   | Samples            |
| Input Range (Differential)                       | IOR On Mode                                                           |     | 3.12 |      | $V_{PP}$           |
|                                                  | IOR Off Mode                                                          |     | 4.6  |      |                    |
| ADC CLK Duty Cycle                               |                                                                       | 20  | 50   | 80   | %                  |
| RMS Clock Jitter                                 | Generated by PLL. Integrated from 0MHz to BWLoop                      |     | 300  |      | fsecond            |
| PLL Loop Filter Bandwidth (BWLoop)               | Low Bandwidth (ADC CLK = 40MHz)                                       |     | 415  |      | KHz                |
|                                                  | High Bandwidth (ADC CLK = 40MHz)                                      |     | 1.5  |      | MHz                |
| Over-sampling Frequency                          |                                                                       | 640 |      | 800  | MHz                |
| Signal-to-Noise Ratio (SNR)                      | 4.4MHz Input, IOR On Mode                                             |     | 67.6 |      | dBFS               |
|                                                  | 4.4MHz Input, IOR Off Mode                                            |     | 69.1 |      |                    |
| Single-Tone SFDR                                 | 4.4MHz Input                                                          |     | 76   |      | dBFS               |
| Signal-To-Noise-and-Distortion (SINAD)           |                                                                       |     | 67   |      | dBFS               |
| Digital Filter Passband                          | ADC CLK = 50 MHz, Ripple < +/-0.01dB                                  |     | 22   |      | MHz                |
|                                                  | ADC CLK = 40 MHz, Ripple < +/-0.01dB                                  |     | 17.6 |      |                    |
| Digital Filter -3 dB Frequency                   | ADC CLK = 50 MHz                                                      |     | 25   |      | MHz                |
|                                                  | ADC CLK = 40 MHz                                                      |     | 20   |      |                    |
| Digital Filter Stop Band Attenuation             | $f_{in} \geq 34.5$ MHz                                                |     | 72   |      | dB                 |
| Digital filter Group Delay                       |                                                                       |     | 19   |      | samples            |
| Digital Filter Group Delay Ripple (peak to peak) | $f_{in} < 22$ Mhz with Equalizer On. See (Note 11)                    |     |      | 0.05 | samples            |
| Instant Overload Recovery (IOR)                  | $\leq 5$ dB above Full Scale (dBFS)                                   |     | 1    |      | Sample Clock cycle |
| Power Consumption (Active)                       | All 8 channels Active (PD = 0) at 40 MSPS (Group Delay Equalizer OFF) |     | 350  |      | mW                 |
|                                                  | All 8 channels Active (PD = 0) at 50 MSPS (Group Delay Equalizer OFF) |     | 385  |      |                    |
|                                                  | All 8 channels Active (PD = 0) at 40MSPS (Group Delay Equalizer ON)   |     | 383  |      |                    |
|                                                  | All 8 channels Active (PD = 0) at 50MSPS (Group Delay Equalizer ON)   |     | 435  |      |                    |
| Power Consumption (Sleep)                        | Sleep mode, all 8 channels. See (Note 5)                              |     | 40   |      | mW                 |
| Power Consumption (Power Down)                   | Power-Down mode, all 8 channels                                       |     | 5    |      | mW                 |
| Recovery Time from CW Doppler Mode               | ADC CW/DVGA pin switch from Hi to LO                                  |     | 170  |      | $\mu\text{s}$      |
| Power-up Time                                    | From single channel Power Down (SPI™ register 01h)                    |     | 6    |      | $\mu\text{s}$      |
|                                                  | From Power Down mode (SPI™ register 00h[0] = HI)                      |     | 20   |      | ms                 |

## Digital Input and Output Characteristics

Unless otherwise noted, specified limits apply ADC AVDD = ADC DVDD = 1.2V; ADC CLK = 40 MHz, ADC IO DVDD = AMP IO DVDD = 1.2V, ADC data out  $R_L$  = 100Ω, SPI™ DIO capacitance = 5pF; **Boldface limits** apply for  $T_A = T_{MIN}$  to  $T_{MAX}$ ; All other limits apply for  $T_A = +25^\circ\text{C}$ .

| Parameter                                                                                                                                                                                            | Conditions                                                                                          | Min        | Typ                   | Max        | Units                |
|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------------------------------------------------------------------------------|------------|-----------------------|------------|----------------------|
| <b>Single Ended I/O: SPI™ CLK, SPI™ DIO, ADC SPI™ CS, AMP SPI™ CS, DVGA CLK, DVGA UP, DVGA INIT MSB, DVGA INIT LSB, CW/DVGA RST, AMP CW/DVGA, ADC CW/DVGA, LNA PD, DVGA PD, AMP RST, DVGA PA HI:</b> |                                                                                                     |            |                       |            |                      |
| <b>Levels &amp; Generic Specifications:</b>                                                                                                                                                          |                                                                                                     |            |                       |            |                      |
| Logical Input "HI" Voltage                                                                                                                                                                           |                                                                                                     | 900        |                       |            | mV                   |
| Logical Input "LO" Voltage                                                                                                                                                                           |                                                                                                     |            |                       | 300        | mV                   |
| Logical Input Current                                                                                                                                                                                |                                                                                                     |            |                       | ±1         | μA                   |
| SPI™ DIO Logical Output "HI" Voltage                                                                                                                                                                 | Test run at 1MHz                                                                                    | 950        | IO DVDD               |            | mV                   |
| SPI™ DIO Logical Output "LO" Voltage                                                                                                                                                                 | Test run at 1MHz                                                                                    |            | 0                     | 250        | mV                   |
| <b>Timing:</b>                                                                                                                                                                                       |                                                                                                     |            |                       |            |                      |
| CW/DVGA RST Setup Time                                                                                                                                                                               | Falling edge must precede CW CLK+ rising transition by ( $t_{CWS}$ ). See <a href="#">Figure 10</a> | 2          |                       |            | ns                   |
| CW/DVGA RST Hold Time                                                                                                                                                                                | Falling edge must follow CW CLK+ rising transition by ( $t_{CWH}$ ). See <a href="#">Figure 10</a>  |            | 0                     |            | ns                   |
| CW/DVGA RST Pulse Width                                                                                                                                                                              | CW Doppler Mode. See <a href="#">Figure 10</a>                                                      | 2          |                       |            | ns                   |
|                                                                                                                                                                                                      | B-Mode                                                                                              | 200        |                       |            |                      |
| CW/DVGA RST Removal time                                                                                                                                                                             | See ( <a href="#">Note 13</a> )                                                                     | 20         |                       |            | ns                   |
| DVGA CLK pin Freq                                                                                                                                                                                    |                                                                                                     |            |                       | 100        | MHz                  |
| DVGA CLK pin Rise and Fall Time                                                                                                                                                                      | See ( <a href="#">Note 11</a> )                                                                     |            |                       | 7          | ns                   |
| DVGA CLK pin Pulse Width                                                                                                                                                                             |                                                                                                     | 4          |                       |            | ns                   |
| AMP SPI™ CS or ADC SPI™ CS Setup Time ( $t_{SSELS}$ )                                                                                                                                                | See <a href="#">Figure 8</a>                                                                        | 15         |                       |            | ns                   |
| AMP SPI™ CS or ADC SPI™ CSHold Time ( $t_{SSELH}$ )                                                                                                                                                  | See <a href="#">Figure 8</a>                                                                        | 3          |                       |            | ns                   |
| AMP SPI™ CS or ADC SPI™ CSHI Time ( $T_{SSELH}$ )                                                                                                                                                    | Read / Write Transactions. See <a href="#">Figure 9</a>                                             |            |                       | 250        | ns                   |
| SPI™ DIO Setup Time ( $t_{WS}$ )                                                                                                                                                                     | Write Transaction. See <a href="#">Figure 8</a>                                                     | <b>110</b> | 40                    |            | ns                   |
| SPI™ DIO Hold Time ( $t_{WH}$ )                                                                                                                                                                      | Write Transaction. See <a href="#">Figure 8</a>                                                     | <b>24</b>  | 40                    |            | ns                   |
| SPI™ CLK Write Period ( $t_{SCLK}$ )                                                                                                                                                                 | Write Clock Period. See <a href="#">Figure 8</a>                                                    | <b>0.2</b> | 1                     |            | μs                   |
| SPI™ Read Propagation Delay ( $t_{OD}$ )                                                                                                                                                             | Read Transaction Propagation Delay. See <a href="#">Figure 9</a>                                    |            |                       | <b>120</b> | ns                   |
| SPI™ Master Hi-Z End ( $t_{HiZ-E}$ )                                                                                                                                                                 | Read Transaction End of SPI™ Master HiZ. See <a href="#">Figure 9</a>                               |            | 100                   |            | ns                   |
| SPI™ Read Valid Time ( $t_{VALD}$ )                                                                                                                                                                  | Read Transaction. See <a href="#">Figure 9</a>                                                      |            | $t_{SCLKRD} - t_{OD}$ |            | ns                   |
| SPI™ CLK Read Period ( $t_{SCLKRD}$ )                                                                                                                                                                | Read Clock Period. See <a href="#">Figure 9</a>                                                     | <b>0.2</b> |                       |            | μs                   |
| SPI™ CLK Duty Cycle ( $t_{SCKL} / t_{SCLKH}$ )                                                                                                                                                       | See <a href="#">Figure 8</a>                                                                        | 45         |                       | 55         | % of SPI™ CLK Period |
| SPI™ CLK Rise / Fall Time ( $t_{SCLKR} / t_{SCLKF}$ )                                                                                                                                                | See <a href="#">Figure 8</a>                                                                        |            | 50                    |            | ns                   |
| <b>Differential Input:</b>                                                                                                                                                                           |                                                                                                     |            |                       |            |                      |
| <b>Levels &amp; Generic Specifications:</b>                                                                                                                                                          |                                                                                                     |            |                       |            |                      |
| CW CLK Level (See <a href="#">Figure 7</a> )                                                                                                                                                         | LVDS, Common Voltage. See ( <a href="#">Note 11</a> )                                               |            | 1.2                   |            | V                    |
|                                                                                                                                                                                                      | LVPECL, Common Voltage. See ( <a href="#">Note 11</a> )                                             |            | 2.0                   |            |                      |
|                                                                                                                                                                                                      | LVDS, Differential Voltage. See ( <a href="#">Note 11</a> )                                         | 240        | 400                   |            | mV                   |
|                                                                                                                                                                                                      | LVPECL, Differential Voltage. See ( <a href="#">Note 11</a> )                                       | 600        | 800                   |            |                      |

| Parameter                                                  | Conditions                                                                        | Min  | Typ             | Max      | Units      |
|------------------------------------------------------------|-----------------------------------------------------------------------------------|------|-----------------|----------|------------|
| CW CLK Input Impedance                                     | Differential                                                                      |      | 10              |          | k $\Omega$ |
| ADC CLK Level                                              | Common Mode (AC Coupled within LM96511). See (Note 16)                            |      | 0.4 to ADC AVDD |          | V          |
|                                                            | Differential Mode Drive (peak-to-peak) or Single Ended. See (Note 16)             | 200  | 400             | ADC AVDD | mV         |
| <b>Differential Output:</b>                                |                                                                                   |      |                 |          |            |
| <b>Levels &amp; Generic Specifications:</b>                |                                                                                   |      |                 |          |            |
| Output Differential Voltage ( $V_{OD}$ )                   | ADC IO DVDD = 1.2V<br>Reduced CM LVDS, RL = 100 $\Omega$ , OCM = 0. See (Note 11) | 318  | 370             | 428      | mV         |
|                                                            | ADC IO DVDD = 1.8V<br>LVDS, RL = 100 $\Omega$ , OCM = 1. See (Note 11)            | 280  | 350             | 417      |            |
|                                                            | ADC IO DVDD = 1.2V<br>SLVS, RL = 100 $\Omega$ . See (Note 11)                     | 262  | 330             | 393      |            |
| Output Common Mode Voltage ( $V_{OCM}$ )                   | ADC IO DVDD = 1.2V<br>Reduced CM LVDS, RL = 100 $\Omega$ , OCM = 0. See (Note 11) | 895  | 945             | 1000     | mV         |
|                                                            | ADC IO DVDD = 1.8V<br>LVDS, RL = 100 $\Omega$ , OCM = 1. See (Note 11)            | 1200 | 1265            | 1340     |            |
|                                                            | ADC IO DVDD = 1.2V<br>SLVS, RL = 100 $\Omega$ . See (Note 11)                     | 185  | 225             | 270      |            |
| Output Short Circuit Current ( $I_{OS}$ )                  | Shorted to GND.                                                                   |      | 4               | 4.5      | mA         |
| High Impedance Output Current ( $I_{OZ}$ )                 | Tri-stated (opened)                                                               | -10  | $\pm 1$         | 10       | $\mu$ A    |
| <b>Timing:</b>                                             |                                                                                   |      |                 |          |            |
| ADC BCLK (Bit Clock) Period ( $t_{BCLK}$ )                 | ADC CLK = 40 MHz. See Figure 5                                                    |      | 4.16            |          | ns         |
| Bit Clock (ADC BCLK) Jitter (RMS)                          | See (Note 11)                                                                     |      |                 | 2        | ps         |
| ADC WCLK (Word Clock) Period ( $t_{WCLK}$ )                | ADC CLK = 40 MHz. See Figure 5                                                    |      | 25              |          | ns         |
| Output Data Edge to Output Clock Edge Setup Time ( $t_s$ ) | ADC CLK = 40 MHz. See Figure 5                                                    | 480  | 900             |          | ps         |
| Output Data Edge to Output Clock Edge Hold Time ( $t_H$ )  | ADC CLK = 40 MHz. See Figure 5                                                    | 770  | 1150            |          | ps         |
| Output Data Valid Window ( $t_{DV}$ )                      | ADC CLK = 40 MHz. See (Note 11) & Figure 5                                        | 1410 | 1820            |          | ps         |
| Rise/ Fall Time                                            | ADC CLK = 50 MHz                                                                  |      | 320             |          | ps         |
| Data Edge to Word Edge Skew ( $t_{DWS}$ )                  | ADC CLK = 50 MHz. See Figure 5                                                    | -720 | -295            | 220      | ps         |
| ADC Input Clock to Word Clock Delay ( $t_{prop}$ )         | ADC CLK = 40 MHz. Upon applying RST signal or a proper power reset.               |      | 5.4             |          | ns         |
|                                                            | ADC CLK = 50MHz. Upon applying RST signal or a proper power reset.                |      | 5.1             |          | ns         |

**Note 1:** Absolute maximum ratings are those values beyond which the safety of the device cannot be guaranteed. They are not meant to imply that the device should be operated at these limits. Operating Ratings indicate conditions for which the device is guaranteed to be functional, but do not guarantee specific performance limits. Guaranteed specifications and test conditions are specified in the Electrical Characteristics sections below. Operations of the device beyond the Operating Ratings is not recommended as it may degrade the lifetime of the device. All voltages are measured with respect to GND = AGND = DNGD = 0V, unless otherwise specified.

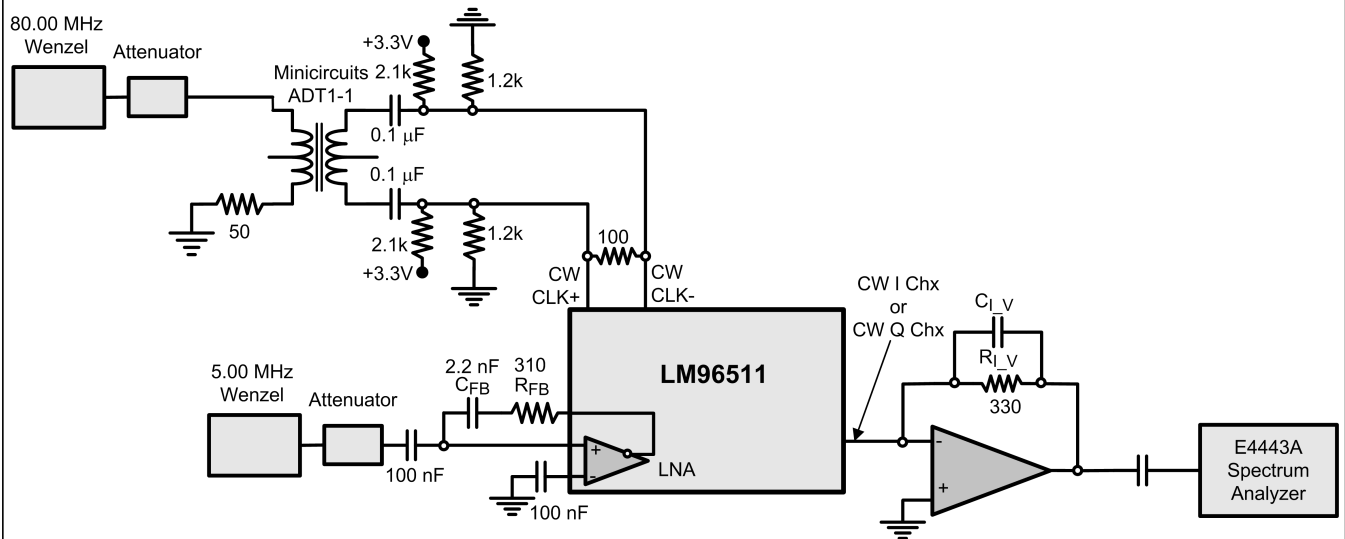
**Note 2:** The LNA non-inverting input is always driven single-ended. The inverting input is always AC grounded. See the Application Information section for typical connection diagrams in Figure 12.

**Note 3:** Min and Max limits are 100% production tested at 25°C. Limits over the operating temperature range are guaranteed through correlation using Statistical Quality Control (SQC) methods. Limits are used to calculate National's Average Outgoing Quality Level (AOQL).

**Note 4:** Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not guaranteed on shipped production material.

**Note 5:** Sleep mode keeps the PLL, Reference and Bias networks active to allow fast recovery and interleaved imaging modes.





$$(1) \text{ Noise (dBc}/\sqrt{\text{Hz}}) = \text{E4443A Noise Marker Reading (dBm/Hz)} * - \text{Full Scale RMS Output (dBm)}$$

\* Reading RSS corrected for CW Doppler Off

$$(2) \text{ Full Scale RMS Output (dBm)} = 20 \times \log \left( \frac{\text{LNA Input (V}_{PP}) \times \text{CW Doppler Gain} \times R_{I\_V}}{2\sqrt{2}} \right) + 13.0$$

CW Doppler Gain = 25.8 mA/V

$R_{I\_V} = 330\Omega$

$$(3) \text{ Full Scale RMS Output (dBm)} = 20 \times \log (\text{LNA Input (V}_{PP}) + 22.6$$

30087090

**FIGURE 4. CW Doppler Phase Noise Measurement**

**Note 22:** Please take note of the LNA Input Amplitude Range information described in the [LNA INPUT AMPLITUDE RANGE](#) Section

## Timing Diagrams

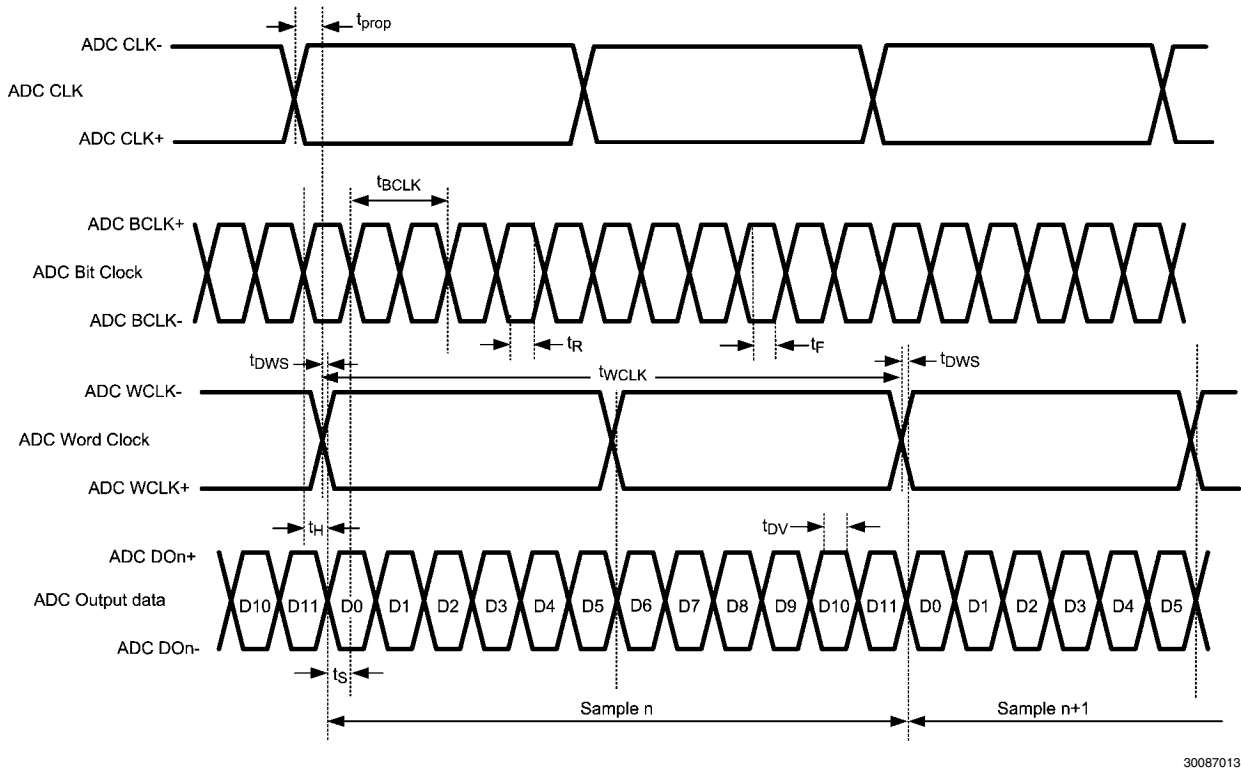


FIGURE 5. B-Mode ADC Data Output Timing

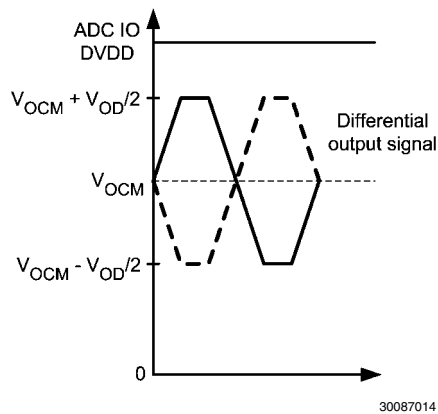


FIGURE 6. B-Mode ADC Data Output Level Definitions

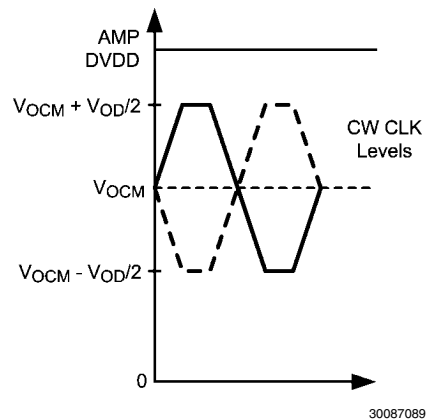


FIGURE 7. CW CLK Level Definitions

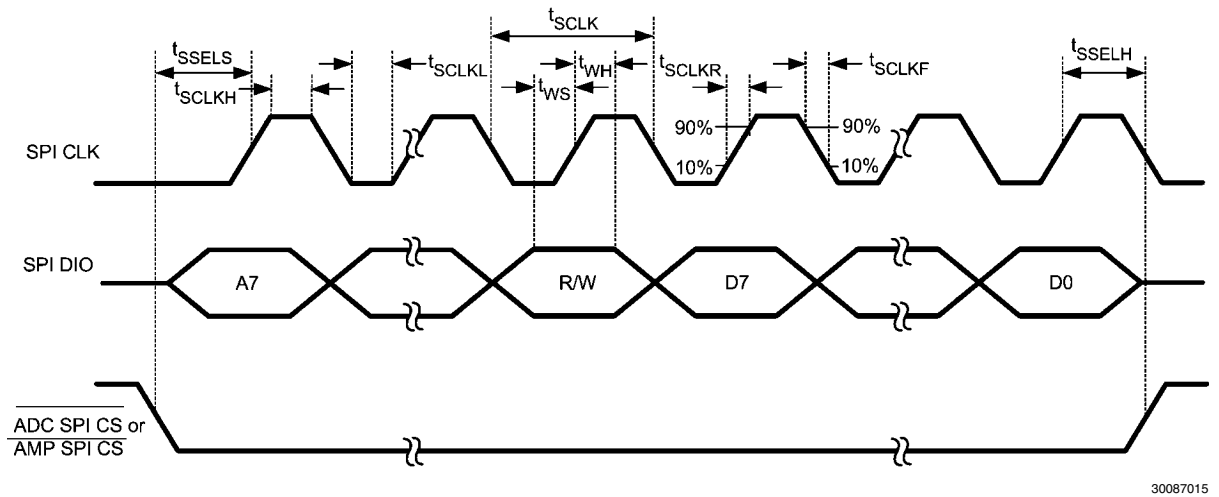


FIGURE 8. SPI™ Write Timing

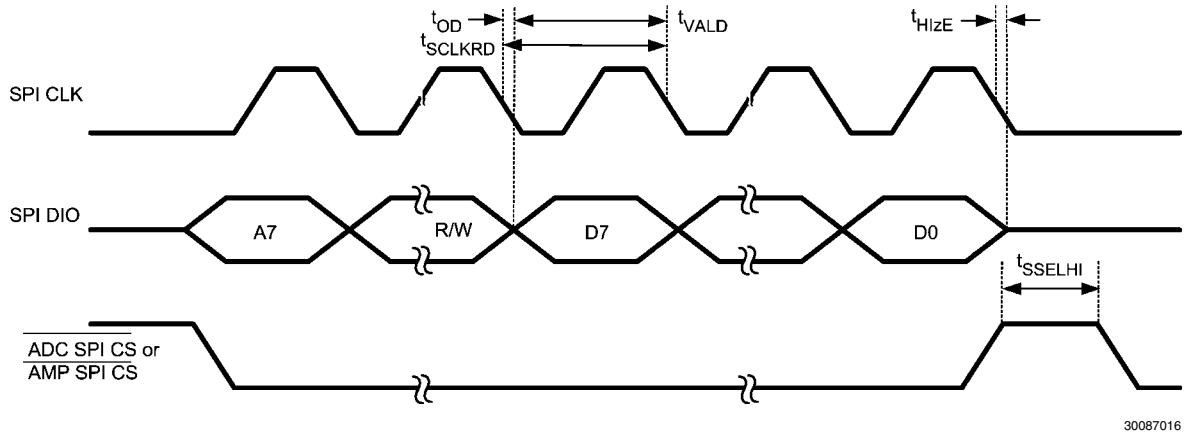


FIGURE 9. SPI™ Read Timing

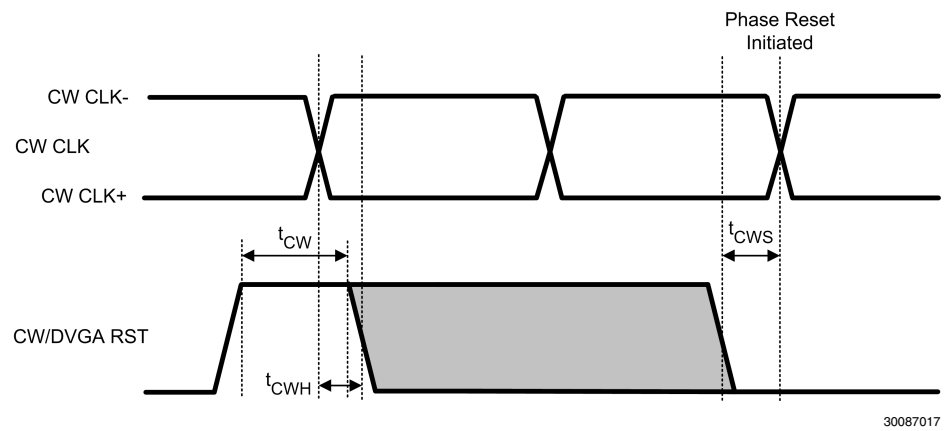
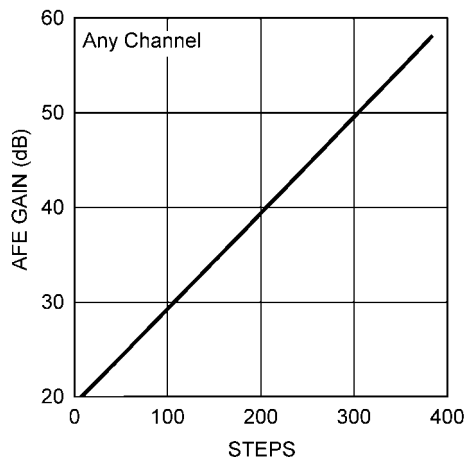


FIGURE 10. CW/DVGA RST Timing (CW Doppler Mode)

## Typical Performance Characteristics

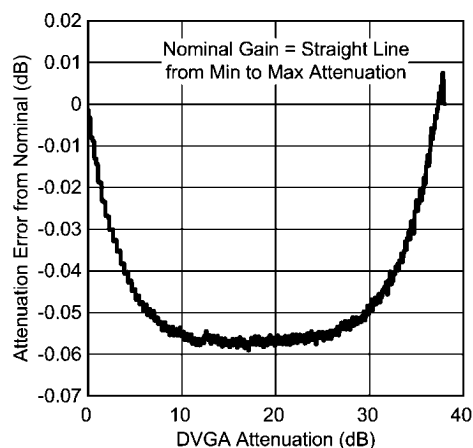
Unless otherwise noted, AMP AVCC A = AMP DVDD = 3.3V, CW AVCC = 5V; ADC AVDD = ADC DVDD = 1.2V, ADC IO DVDD = AMP IO DVDD = 1.2V, Full Scale RF Input at 5 MHz; CW CLK = 80 MHz;; FCLK = 40 MSPS ,TA = +25°C.

**AFE Gain vs. Steps (DVGA PA HI = HI)**



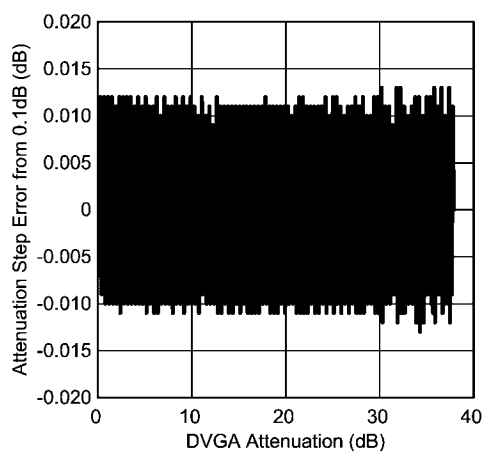
30087024

**Attenuation Error from Nominal**



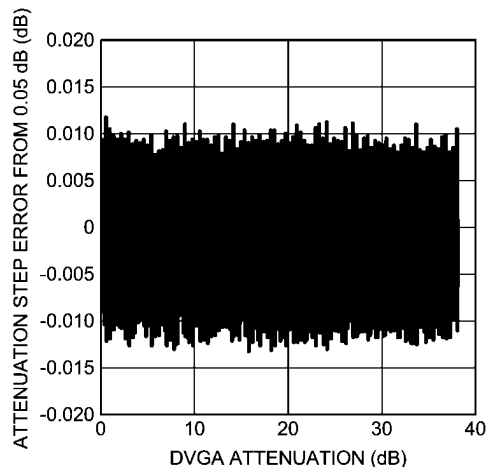
30087063

**Attenuation Step Error from 0.1 dB**



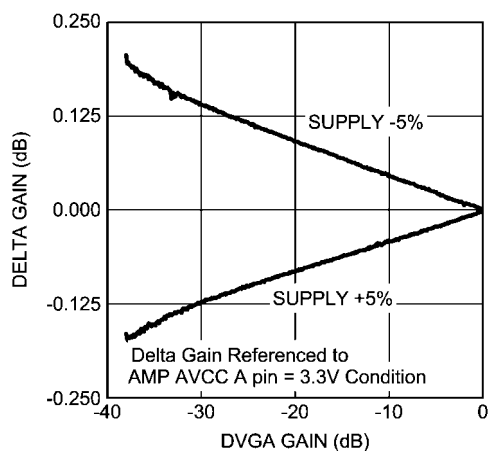
30087064

**Attenuation Step Error from 0.05 dB**



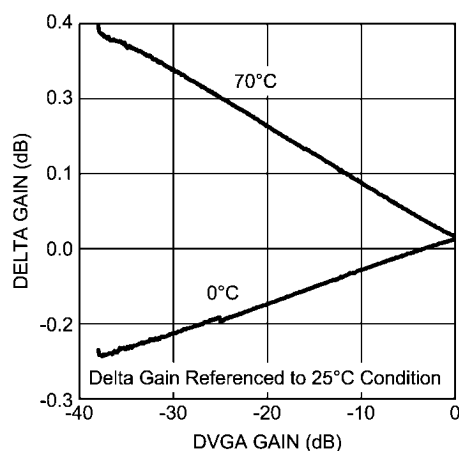
30087088

**Gain Variation from Nominal vs Supply Voltage**

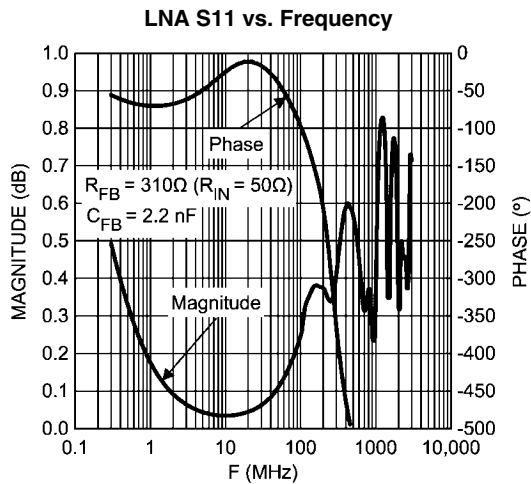


30087027

**Gain Variation from Nominal vs Temperature**

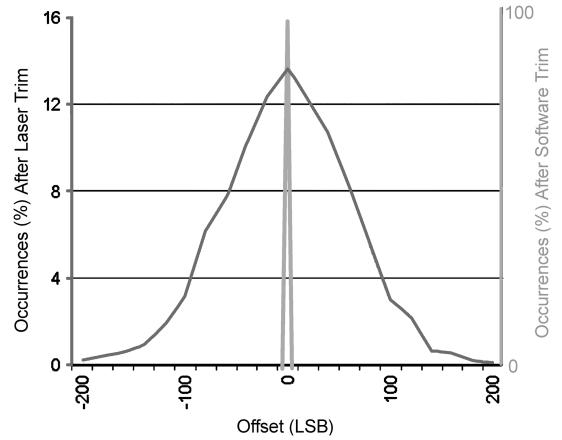


30087026

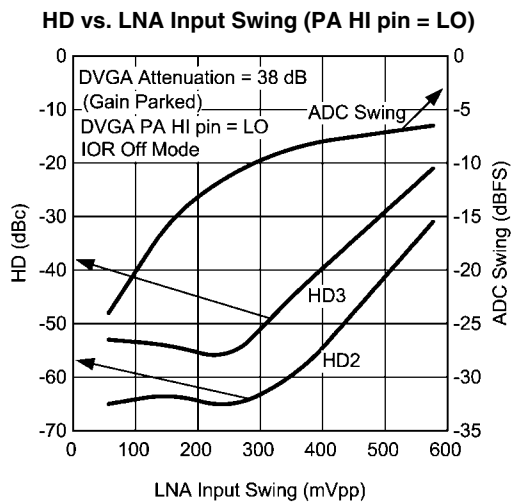


30087067

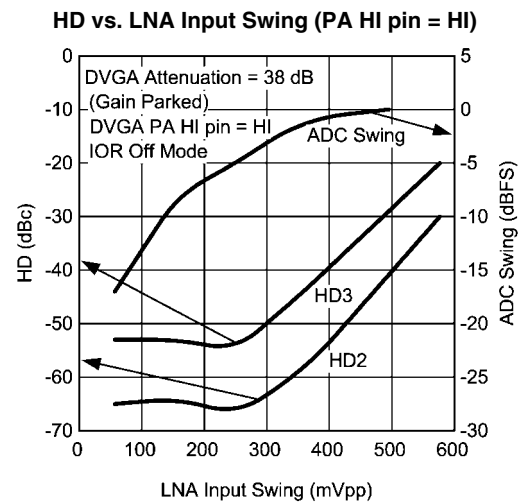
**AFE Offset Distribution IOR On Mode, Minimum DVGA attenuation, DVGA PA HI pin = LO**



30087092

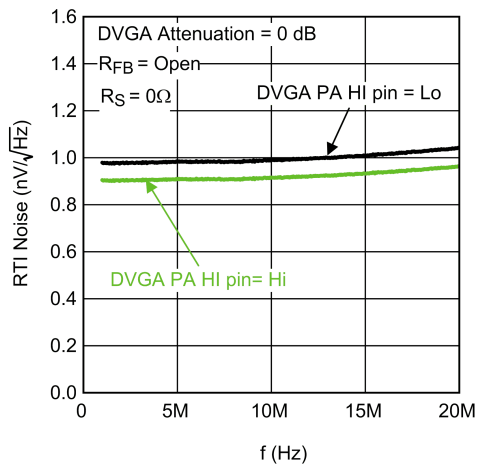


30087091



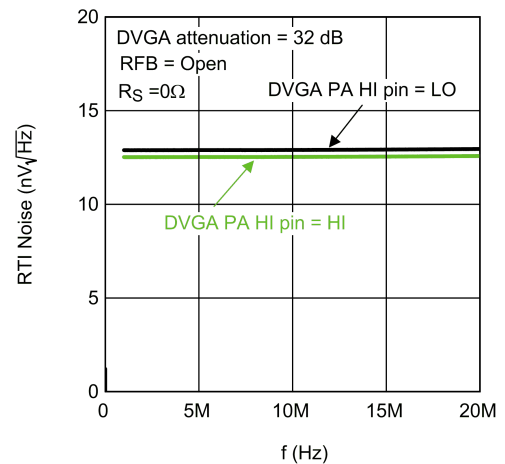
30087093

**RTI Noise vs. Frequency (DVGA Attenuation = 0dB)**



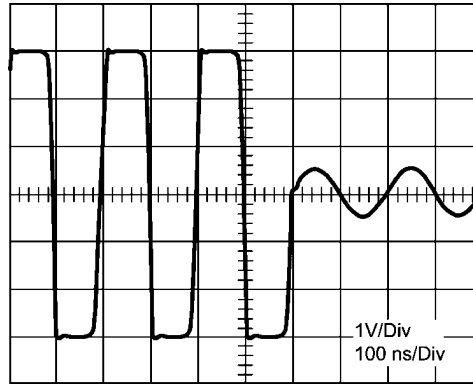
30087022

**RTI Noise vs. Frequency (DVGA Attenuation = 32dB)**



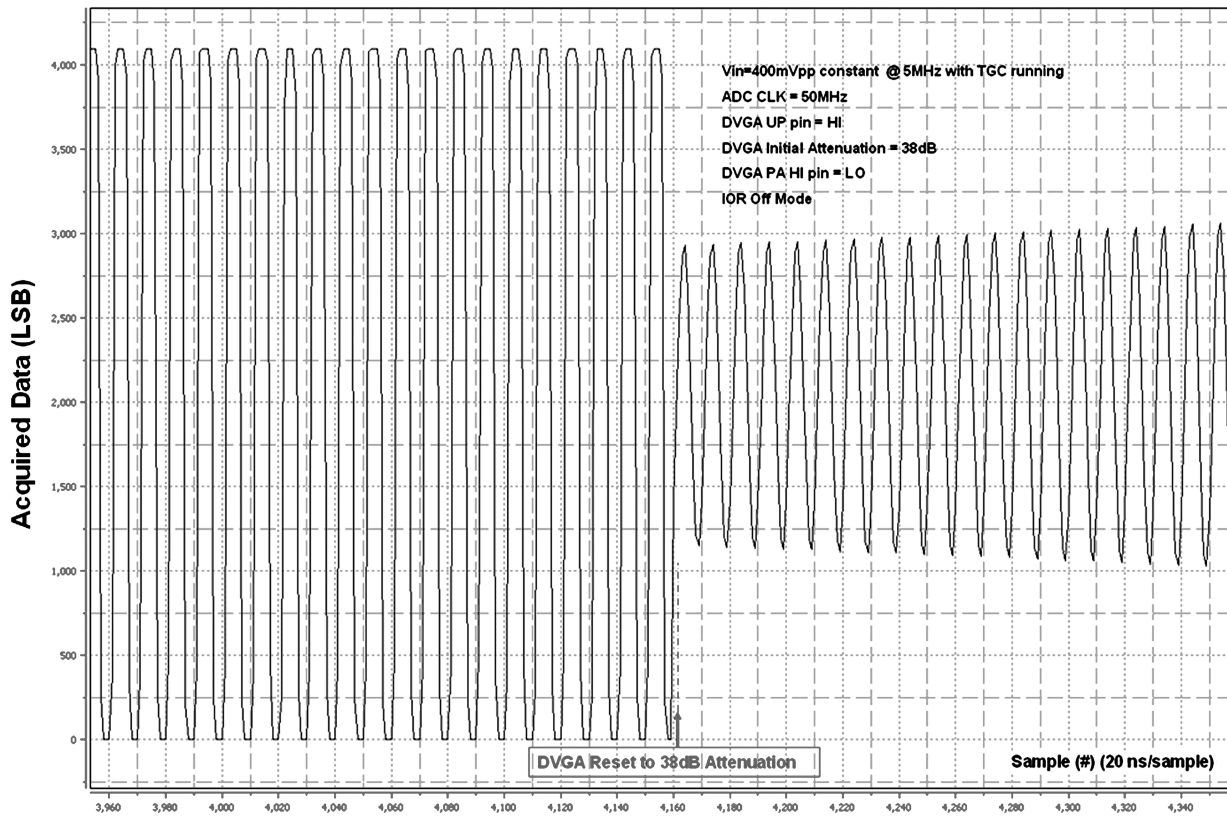
30087082

### Far-Field Overload Recovery @ Post Amp Output (No User Access)



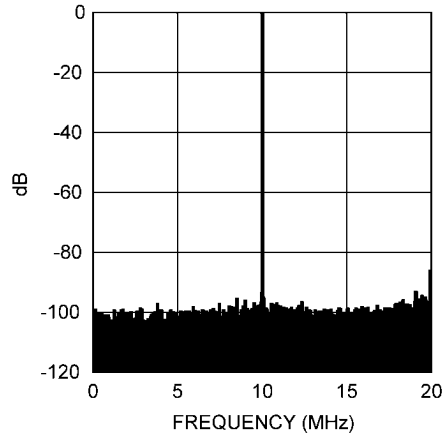
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### AFE (B-Mode) Overload Recovery



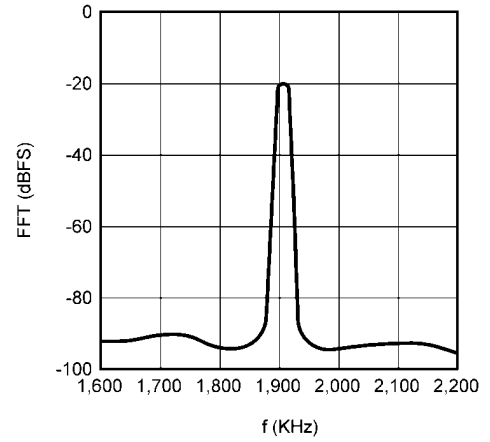
30087094

**Spectral Response @  $f_{IN}=10$  MHz,  
ADC CLK = 400 mHz, IOR On**



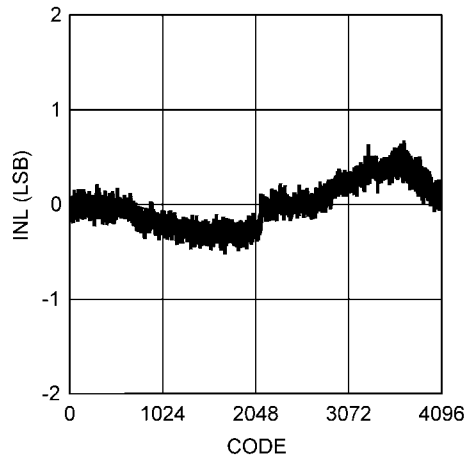
30087077

**Close-In Spectral Response @  $f_{IN}=1.9$  MHz,  
TGC Running, Cosine 6 Term Window**



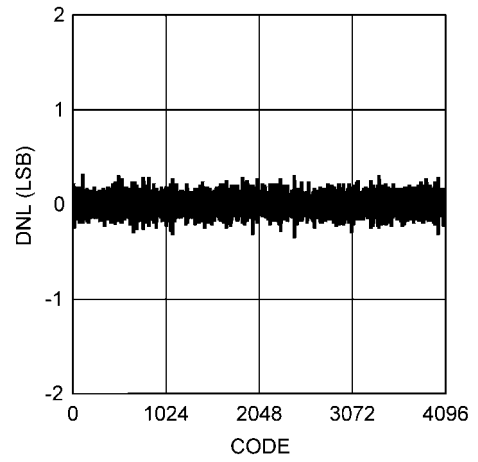
30087095

**ADC INL**



30087076

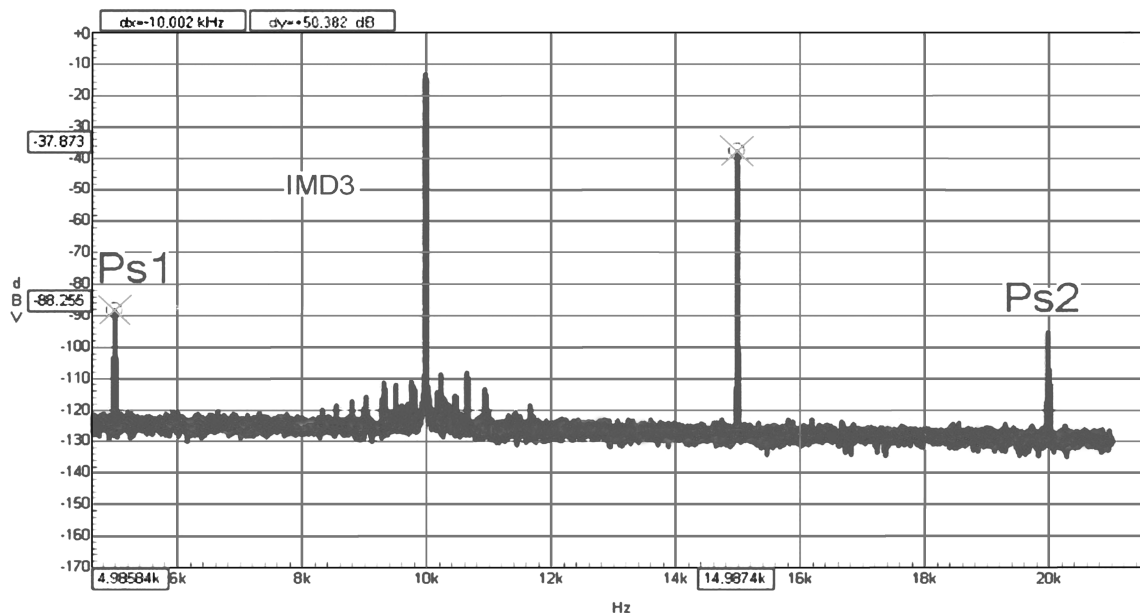
**ADC DNL**



30087075

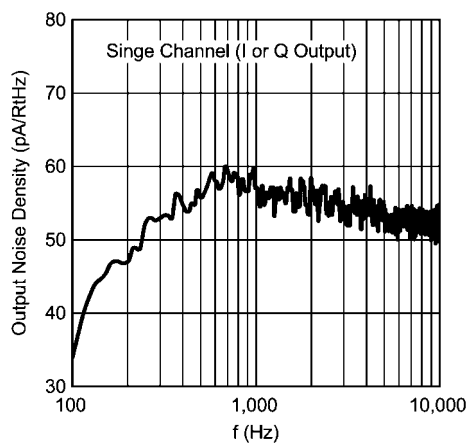
## CW Doppler Plots

CW Doppler IMD3, Unequal Tones  
See Electrical Characteristics (Note 13),  
10kHz & 15kHz Offset,  
25 dB Separation



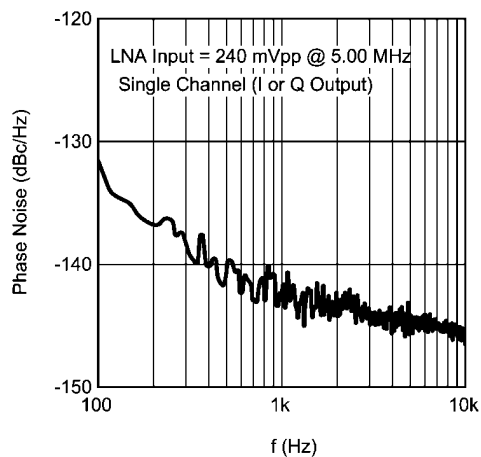
30087030

CW Doppler Output Noise (CWDIFF CLK = 80.0MHz)



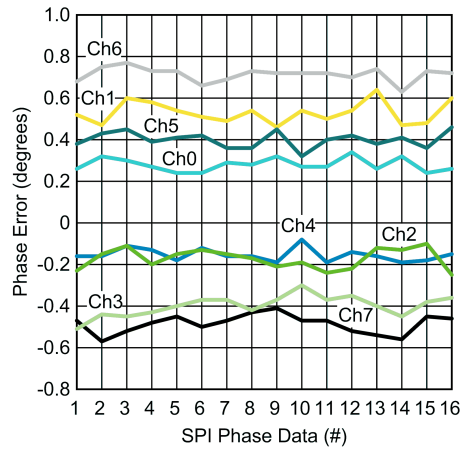
30087080

CW Doppler Phase Noise,  
See Electrical Characteristics (Note 6)



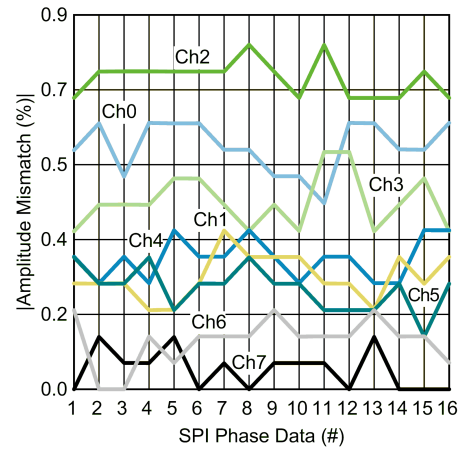
30087081

I-Q Quadrature Phase Error (Within Channel)



30087068

I-Q Output Amplitude Match (Within Channel)



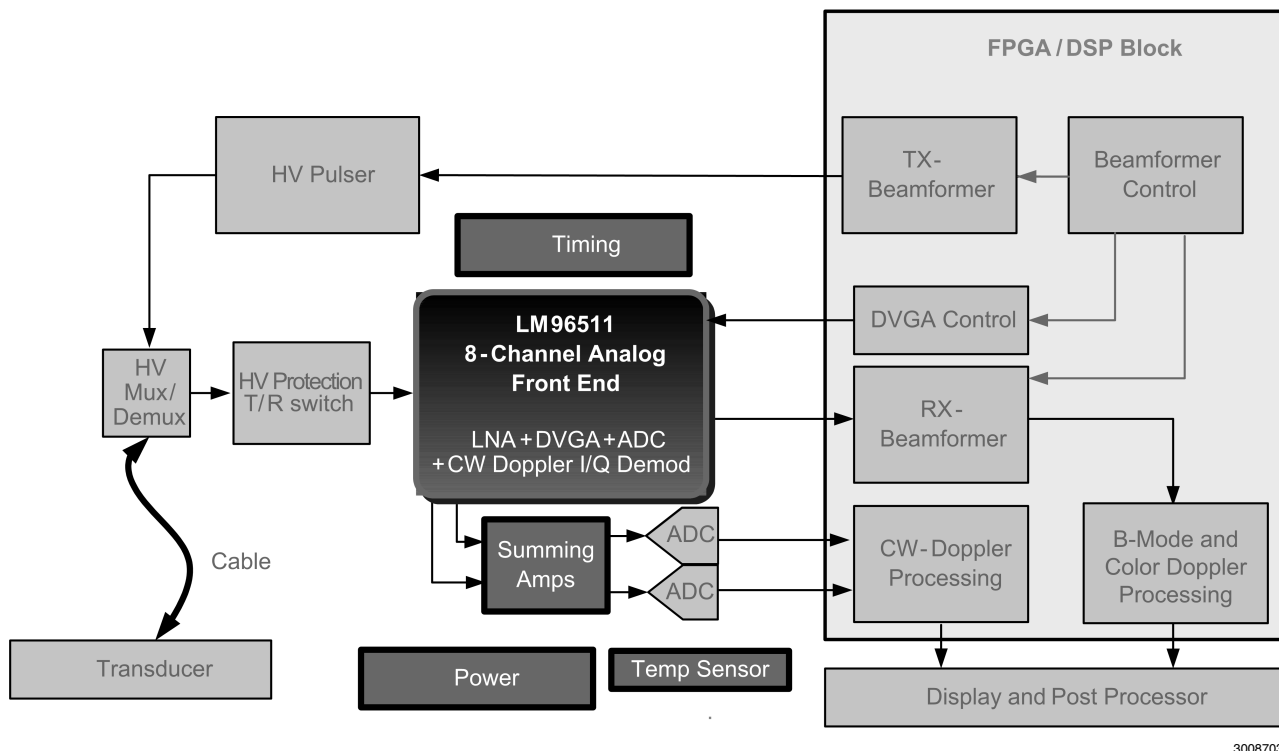
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## Overview

The LM96511 is an eight-channel, fully integrated entire sub-system intended for ultrasound receive applications. LM96511 consolidates many receiver functions currently residing in multiple IC's, thereby achieving lower cost, higher board density, higher performance, lower system integration cost, and lower power consumption. The LM96511 has two distinct signal paths: one for B-mode (Brightness) and the other for CW-mode (CW Doppler). The LM96511 consists of the following blocks / functions for each of its 8 channels:

1. Low-Noise Amplifier (LNA) with programmable input impedance for improved ultrasound probe matching characteristics

2. Digital Variable Gain Amplifier (DVGA) with capability to increase or decrease gain (linear in dB) using digital input for rate of change control
3. 12-Bit ADC with on board PLL for superior jitter reduction
4. CW Doppler output (I and Q) with 16 user selectable phase rotation
5. SPI™ compatible interface for user programming and control



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FIGURE 11. Ultra-Sound System Block Diagram

### LNA INPUT AMPLITUDE RANGE

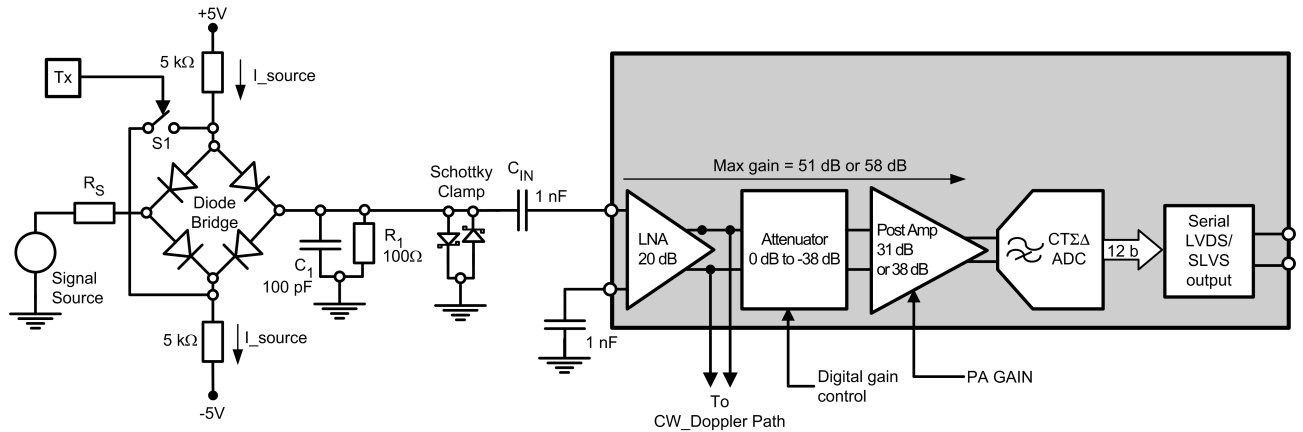
The input amplitude range of the LM96511's Low Noise Amplifier is well suited for ultrasound applications in both CW and B-Mode operation. However, T/R switch leakage and strong echoes from near-field or acoustically dense material is unavoidable. Because of such large transient signal amplitudes and increasing DVGA gain during TGC, overload at the LNA input impairs signal integrity in ultrasound applications. Thus, it is very important to prevent the LM96511 inputs from being overloaded by: (1) limiting the input signal amplitude (see further explanation in the next section); (2) gating the transmit signal path before it reaches the T/R switch; and (3) clamping the input signal with a pair of back-to-back signal diodes as additional protection against overload at the LNA input.

Furthermore, in B-Mode TGC operation, when the LNA functions in series with the DVGA and Post-Amplifier, the maximum input signal swing is subject to the LNA's output slew rate limitation. Because the LNA has a maximum differential output slew rate of 100V/μs, or 50V/μs at its inverting output, the input signal should be adjusted such that the inverting

output of the LNA does not exceed this 50V/μs limit. In addition to limiting the input signal slew rate, to avoid further overload effects induced by surges in input bias current associated with the maximum slew rate limitation, the signal swing at the LNA input should be limited to 200mV<sub>PP</sub> for optimal performance across typical signal frequencies above 5MHz. Ultimately, it is most important to ensure that the input signal is within the LNA's slew rate limitation. Thus, as shown in and explained further in the next section, the input circuit to the LM96511 should have the current source for the T/R switch diode bridge carefully selected to limit the input current to the LNA (~1mA) and include a capacitor (~100pF) and resistor (~100Ω) to ground.

### TYPICAL INPUT CONFIGURATION

The schematic in Figure 12 shows a typical B-Mode input configuration circuit for the LM96511. The input is typically AC coupled through a T/R switch diode bridge configuration which blocks the transmit (Tx) high voltage pulses from the receive (Rx) low voltage inputs.



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**FIGURE 12. Signal Path (B-Mode) Single Channel Including Input Clamp and Diode Bridge**

It is recommended to use National Semiconductor's LM96530 T/R switch with the LM96511 AFE for optimal operation and performance. Alternatively, the discrete 4-diode bridge T/R switch shown in [Figure 12](#) may be used. In such designs, diode characteristics are not ideal, and thus the LM96511 inputs should be protected from the resulting leakage transients, as well as strong reflections. Thus, the transmit signal path should be gated off with switch S1.

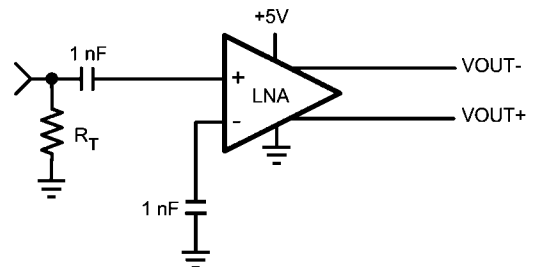
During Ultrasound Rx, switch S1 is open and, with no input signal, "I\_source" flowing from the top current source, through the 4 diodes, to the bottom current source. The Input signal crosses the diode bridge to the LM96511 input as long as the current through  $C_{IN}$  is less than "I\_source" (~1mA). Larger input signal amplitudes which require excess  $C_{IN}$  current beyond I\_source's value will thus be limited by the diode bridge action. During the Tx cycle, switch S1 is shorted so that the Diode Bridge is current starved and any leakage from the T/R switch (not shown) will be strongly attenuated. This ensures effective isolation for maximum protection in the presence of any Tx leakage.

In addition to gating the transmit path with switch S1, capacitor C1 and termination resistor R1 must be included to improve overload recovery time and reduce reflection. C1 acts as a filter to suppress high voltage transient spikes, while R1 acts to divide the signal amplitude down to a favorable level for the LM96511 input, e.g., 200mV<sub>PP</sub>. This provides adequate protection for the LNA input. C1 (~100pF) also acts to band-limit the input signal to ensure that it is within the LNA's slew rate limitation. Although R1 may increase the noise figure and the input impedance seen by the ultrasound transducer, it still provides good harmonic distortion and low offset. Finally, the Schottky clamp diodes provide an additional level of overload protection where the LM96511 input swing is limited to ~ ± 0.35V regardless of the LM96511's input impedance.

### PROGRAMMABLE INPUT IMPEDANCE & LNA GAIN SELECTION

The LM96511 input termination can be configured in either of two ways:

**1. Standard Termination** is illustrated in [Figure 13](#), where the receive (Rx) probe (through the T/R switch) is terminated with  $R_T$  for proper cable termination, and AC coupled to the LNA's non-inverting input. The inverting input is returned to ground through a capacitor.



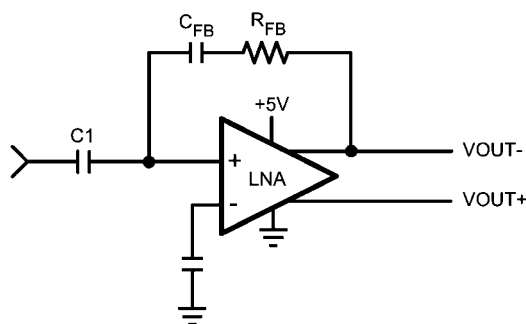
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**FIGURE 13. Standard Input Termination**

**2. Active feedback termination** is illustrated in [Figure 14](#), where no termination resistor is used and feedback ( $R_{FB} + C_{FB}$ ) sets the effective input impedance to provide proper cable termination. This termination scheme is employed for improved harmonic distortion and noise performance. With no physical termination resistor, there is no resistor thermal noise degradation of the LNA noise, and thus increased SNR compared to standard termination.

However, as with any amplifier with active feedback termination, abrupt increases in input amplitude may diminish the active termination and may even result in total loss of termination, which will then further overload the LM96511 inputs. It is important to be mindful that with active feedback termination, the LNA is: (1) even more susceptible to overload effects associated with the maximum slew rate limitation mentioned above; and (2) subject to gain reduction at higher output amplitudes. Thus, in achieving better harmonic distortion and noise performance, active feedback termination may be employed, but as long as the input signal is limited to an

amplitude of  $200\text{mV}_{\text{PP}}$  and slew-rate limited such that the LNA inverting output slew rate is less than  $50\text{V}/\mu\text{s}$ .



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**FIGURE 14. Active Termination Schematic**

Active impedance termination is achieved through an external shunt feedback resistor from LNA IN+ to LNA OUT-. The input resistance  $R_{\text{IN}}$  is given by the equation below, where  $A$  is the LNA single-ended gain ( $=10\text{V}/\text{V} \div 2 = 5\text{V}/\text{V}$ ) and  $5\text{k}\Omega$  is the un-terminated input impedance of the LM96511 LNA.  $C_{\text{FB}}$  is required in series with  $R_{\text{FB}}$ , since the DC levels at LNA IN+ and LNA OUT- are unequal.

$$R_{\text{IN}} = \frac{R_{\text{FB}}}{1 + A} \parallel 5\text{ k}\Omega$$

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| $R_{\text{IN}} (\Omega)$ | $R_{\text{FB}} (\Omega)$ |
|--------------------------|--------------------------|
| 50                       | 301                      |
| 7                        | 453                      |
| 100                      | 619                      |
| 200                      | 1.24k                    |
| 1k                       | 7.5k                     |
| 3k                       | 45.3k                    |

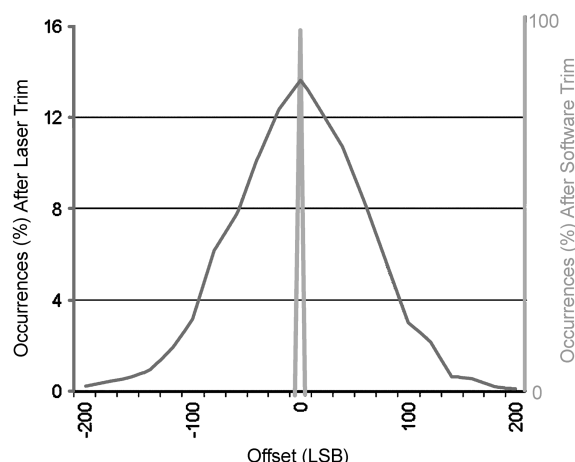
#### OFFSET SOFT-TRIM

To minimize offset, the LM96511 is laser trimmed during manufacturing. To improve accuracy and to allow periodic calibration, if needed, the LM96511's LNA and Post-Amplifier (PA) include provisions for offset trim using the SPI™ compatible interface after chip power-up (volatile).

In B-mode, LNA offset trim improves gain-dependant offset shift, while PA offset trim reduces fixed offset to maximize the LM96511 ADC's Full-Scale swing for maximum dynamic range. SPI™ offset trim should be performed with a software algorithm (Soft-Trim) that looks at the ADC code, at various DVGA attenuation settings, and then invokes a binary search for the best value that centers the ADC code. A couple of it-

erations are usually adequate to “zero-in” on the best Soft-Trim setting for each channel. National Semiconductor provides such software algorithms to its customers for use “as-is” or for modification to meet individual requirements.

Figure 15 shows the LM96511 B-mode offset, measured through the ADC. As can be seen, Soft-trim allows extremely accurate offset adjustment (typically within 1LSB) and allows significant tightening of the distribution.



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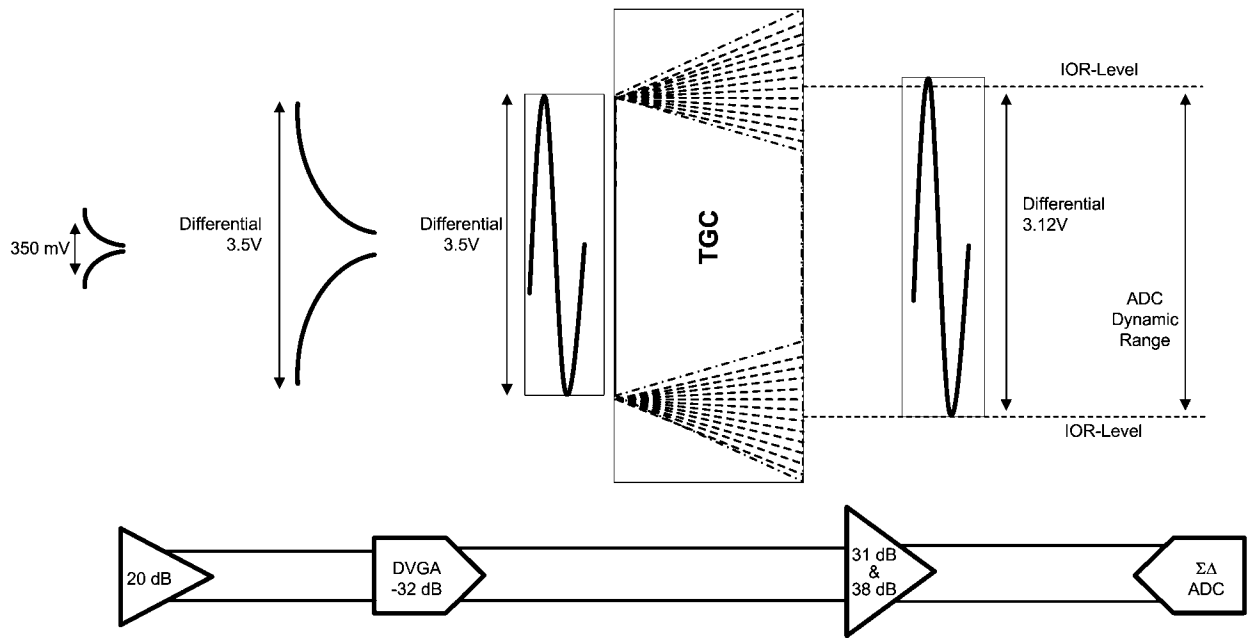
**FIGURE 15. Offset Distribution Histogram including Soft-Trim Improvement**

Maximum expected full scale amplitude loss due to DC offset is:

$$= 20 \times \log \left( \frac{2^{12} - |\text{Offset (LSB)}|}{2^{12}} \right)$$

#### DYNAMIC RANGE

Figure 15 shows the LM96511 B-mode TGC in action. In this diagram, a 5MHz ultrasound signal enters the LNA with  $350\text{mV}_{\text{PP}}$  single ended Near Field (NF) amplitude and the signal path headroom runs into clipping.  $3.5\text{V}_{\text{PP}}$  differential NF amplitude appears at the LNA output (Differential gain = 20dB) where the DVGA TGC will equalize the signal so that the ADC FS range of  $3.12\text{V}_{\text{PP}}$  (with IOR On or  $4.4\text{V}_{\text{PP}}$  with IOR off) can be transversed to maximize the data acquisition resolution. Note that the LM96511's B-mode ADC operates off a 1.2V supply and yet can accommodate  $3.12\text{V}_{\text{PP}}$  FS with IOR on or  $4.4\text{V}_{\text{PP}}$  FS with IOR off. This is because of the coupling resistor ladder built into the ADC in spite of ADC input noise level performance which does not impact ENOB.



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FIGURE 16. LM96511 in Typical TGC Operation at 5MHz

#### DVGA OPERATION

The LM96511 features a linear-in-dB, digital variable gain amplifier which consists of a digitally variable attenuator and post amplifier. The attenuator has a variable range of 0 to -38dB (or -36, -34, or -32dB depending on settings) in increments of either 0.05dB or 0.1dB per LSB step (depending on the "Half Step" mode setting). The variable gain operation is essentially achieved with a "Clock and Reset" scheme. There are three digital control signals for the attenuator: DVGA CLK, CW/DVGA RST, and DVGA UP.

The heart of the variable gain control lies in the DVGA CLK and CW/DVGA RST logic input signals, as illustrated in [Figure 17](#). The positive edge of every CLK pulse will increment or decrement each gain step for as long as the CW/DVGA RST logic pulse is LOW. For a periodic gain ramp-up sequence, the negative edge of every CW/DVGA RST pulse begins a

ramp upwards, and the positive edge of every RESET pulse ends the ramp, resetting the gain back to its DVGA Initial Attenuation. The number of DVGA CLK pulses during each LOW interval of the CW/DVGA RST pulse, determines the duration of the gain ramp, while the frequency of the DVGA CLK pulses determines the slope of the gain ramp.

The DVGA UP input determines whether gain is incremented or decremented. Depending on the logic level of this input, the DVGA can begin at the bottom of the gain ramp (maximum attenuation setting) and proceed to ramp up, or at the top of the gain ramp (minimum attenuation setting) and proceed to ramp down. [Figure 18](#) illustrates how this logic level can also be dynamically changed midway through a ramp up or ramp down operation, which can allow the sonographer to flatten the image's grey background or to reduce the level of a bright reflector.

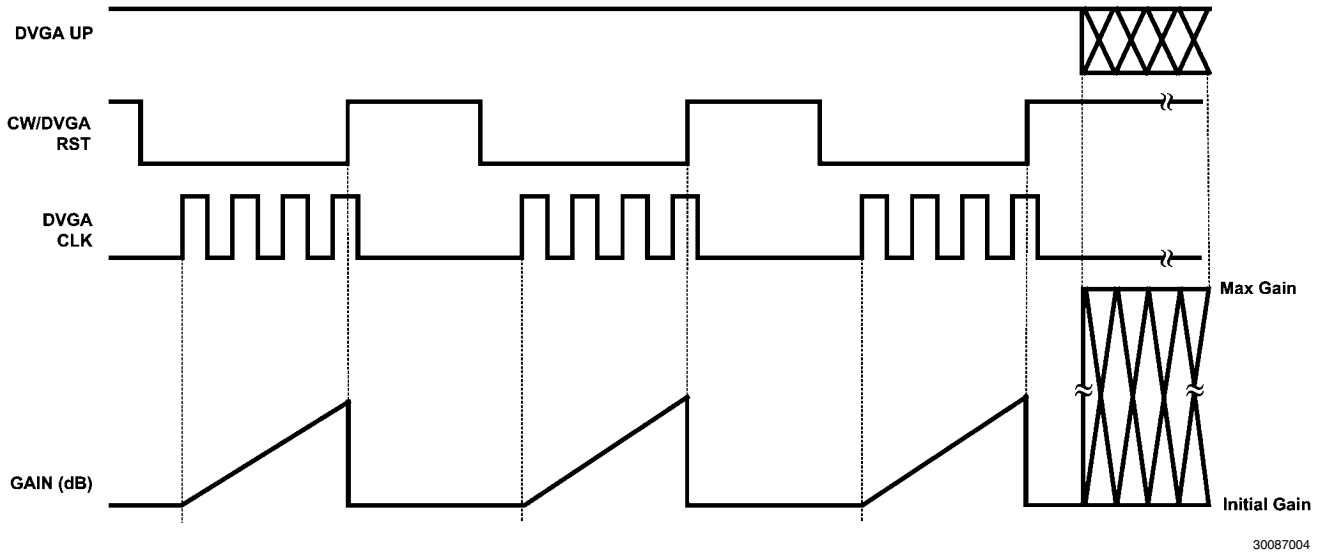


FIGURE 17. Periodic TGC Ramp: Example 1 (Half-Step Disable bit = 1)

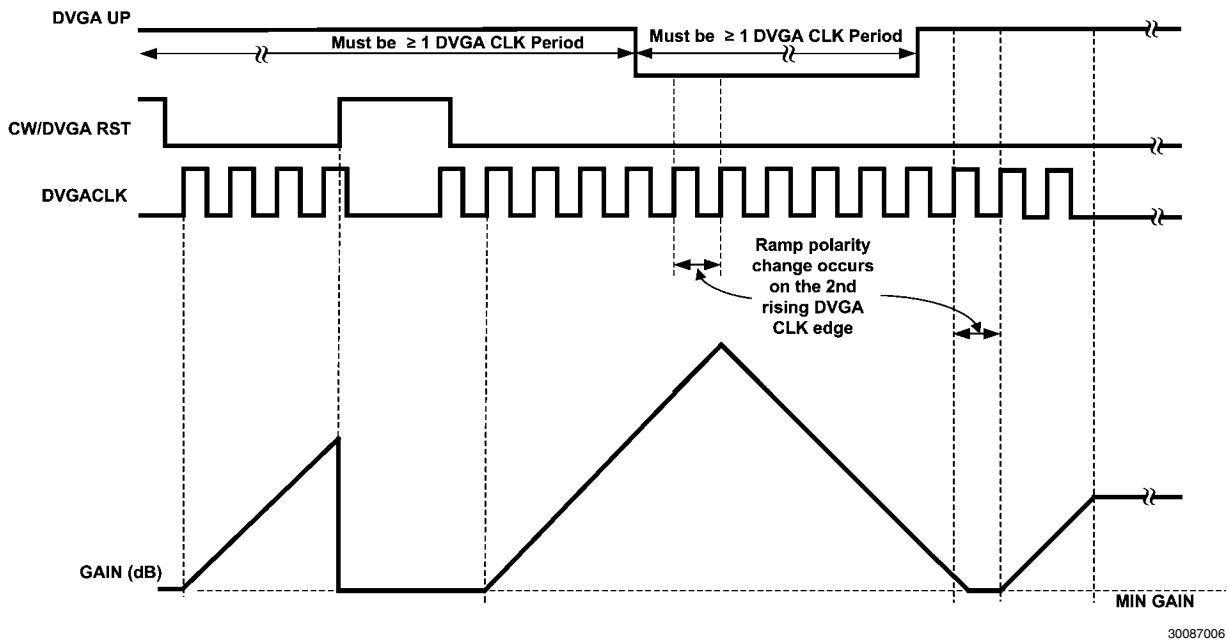


FIGURE 18. DVGA UP bit Change (Half-Step Disable bit = 1)

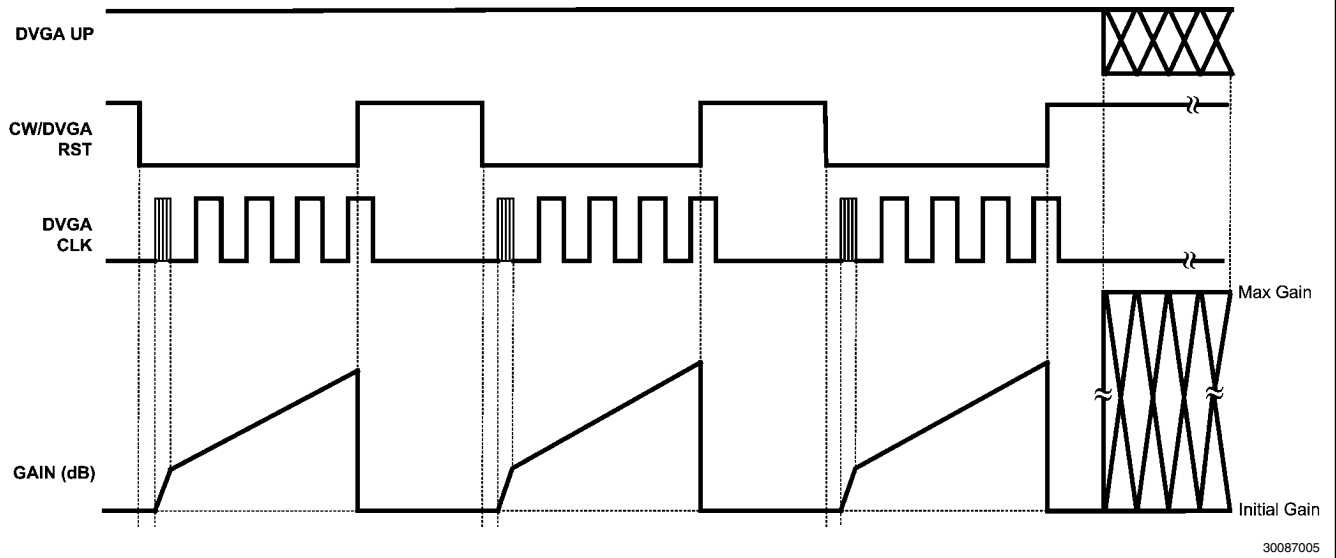


FIGURE 19. Periodic TGC Ramp: Example 2 (Half Step Disable bit = 1)

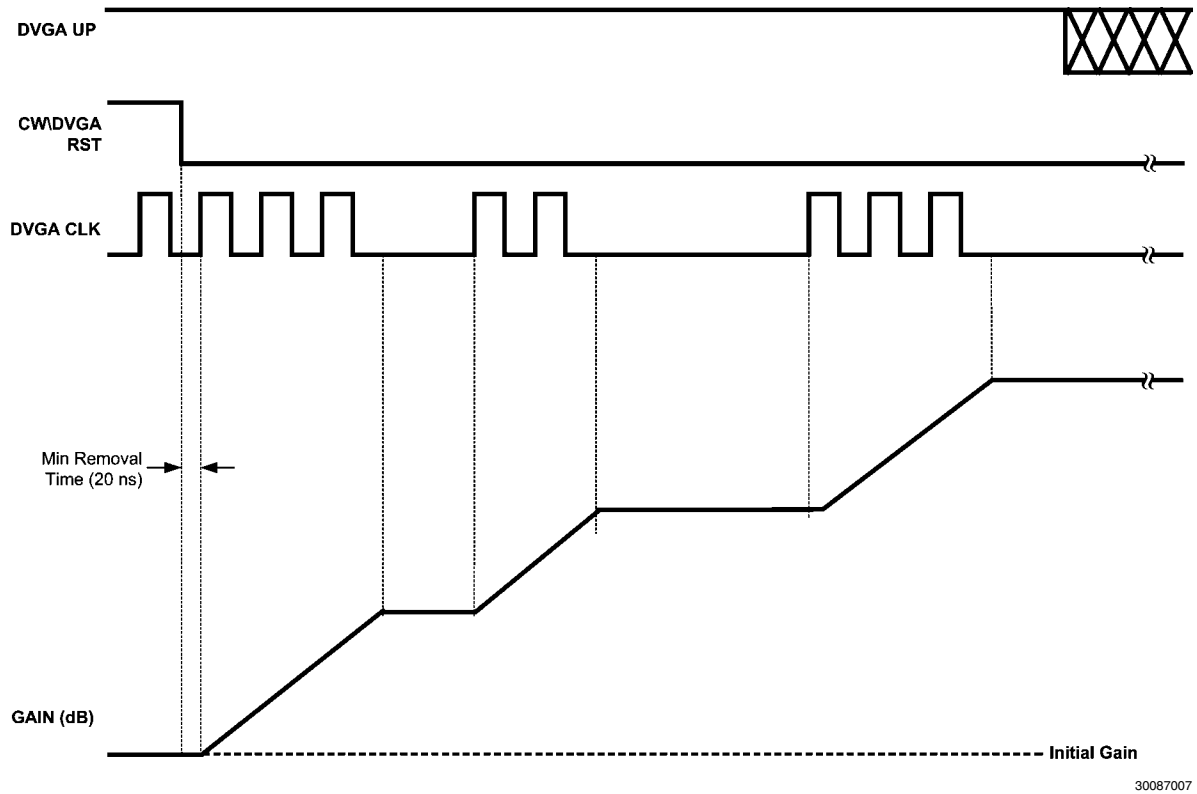


FIGURE 20. Basic Gain Adjustment (Half Step Disable Bit = 1)

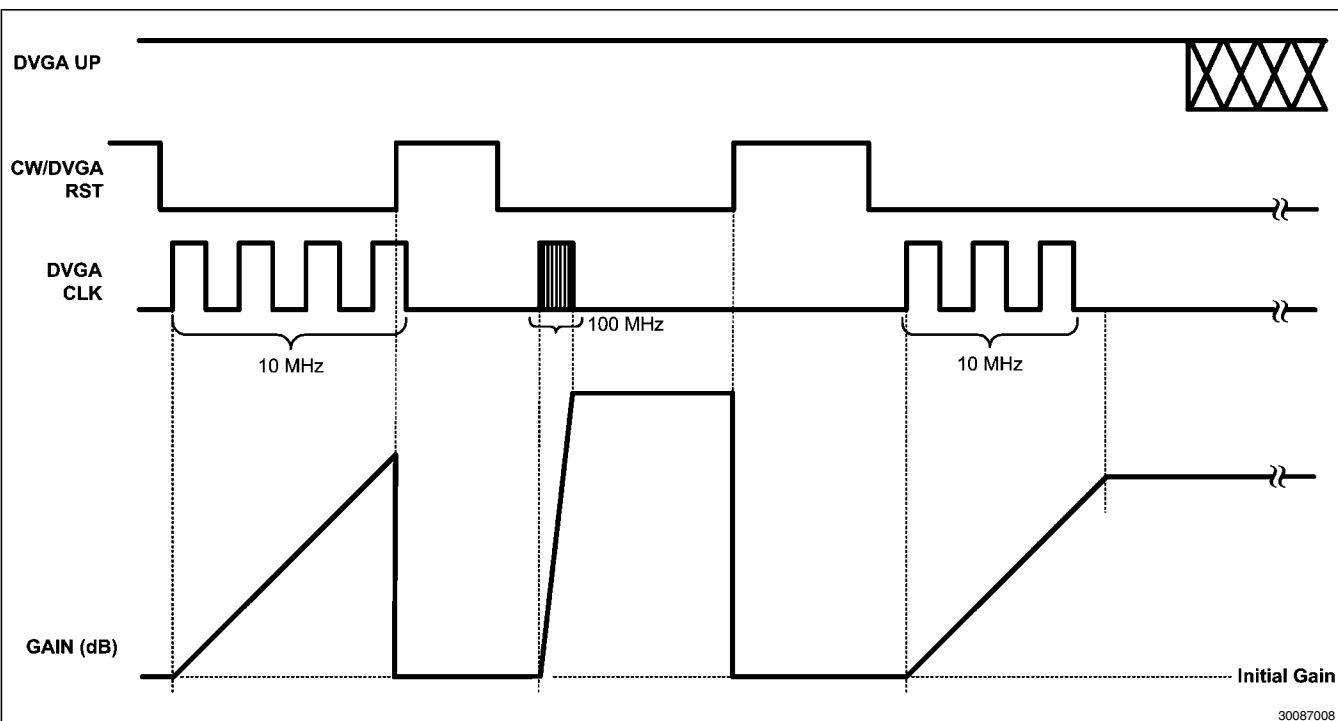


FIGURE 21. Accelerated Gain Adjustment (Half Step Disable bit = 1)

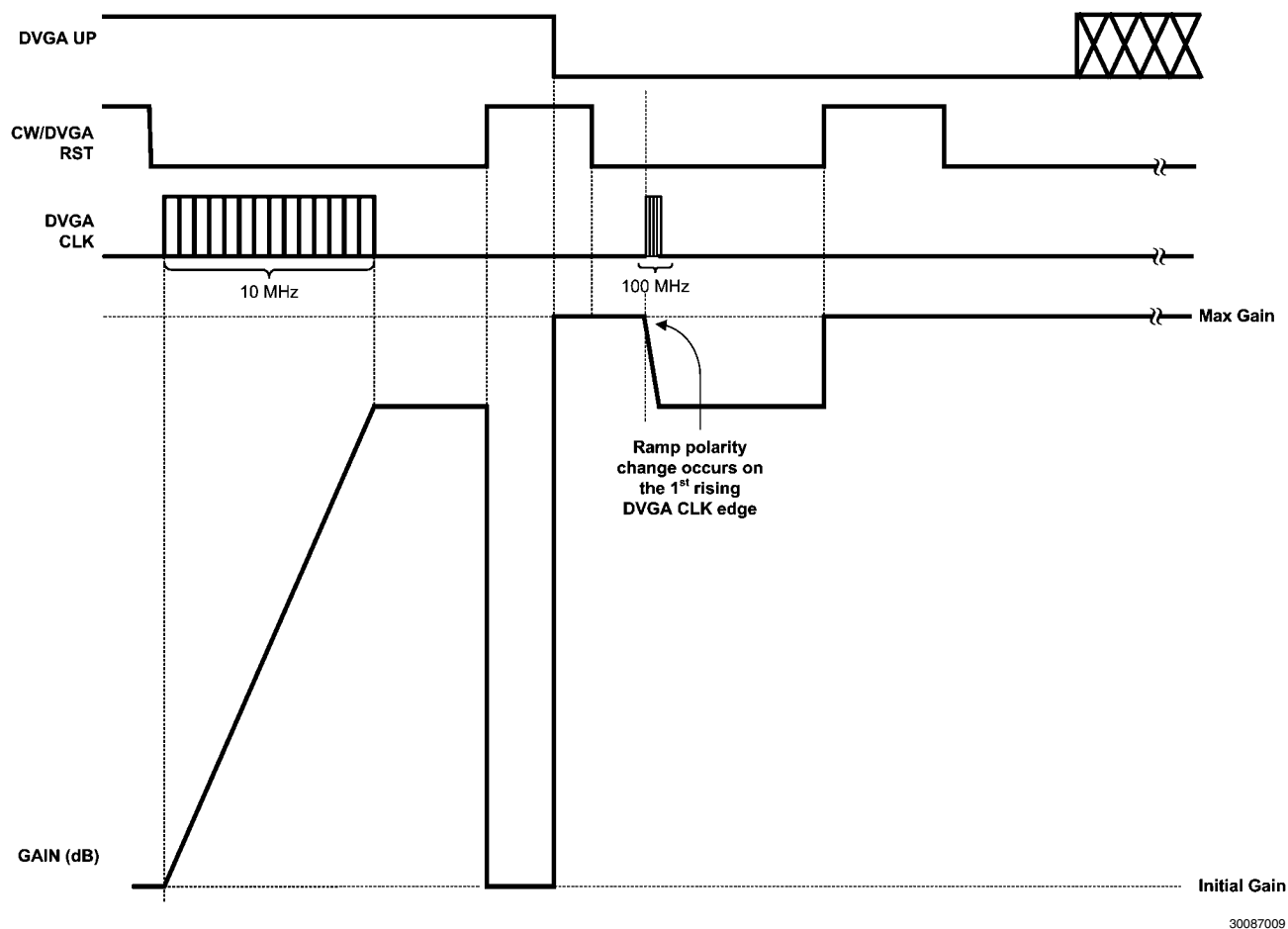


FIGURE 22. Gain Reset with DVGA UP bit = 0

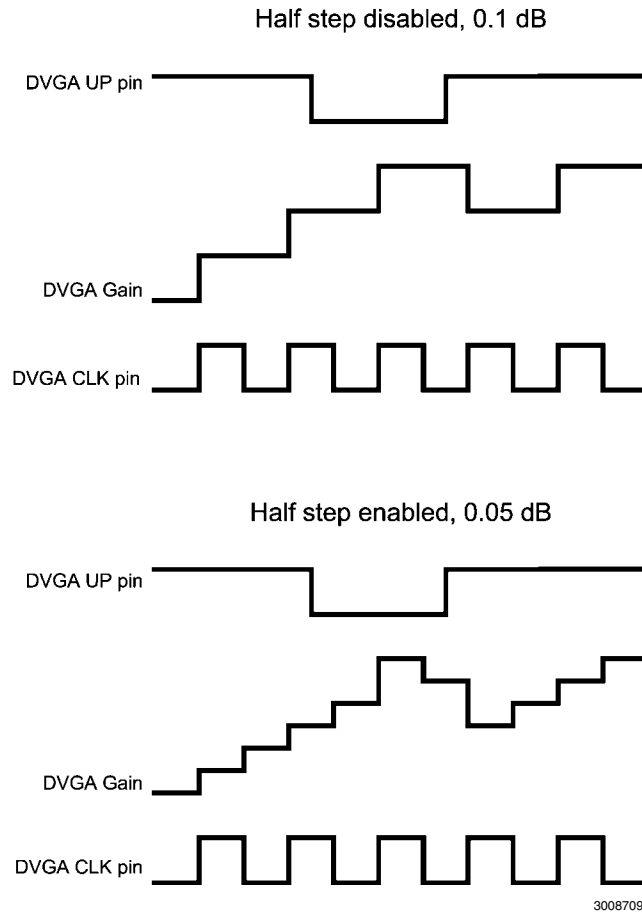


**FIGURE 23. DVGA Gain control “Micro Illustration” of the Gain Stair Case**

#### DVGA Half Step Mode

Another feature of the DVGA which makes it ideal for TGC (Time Gain Control) Applications is its ultra-fine gain step resolution. In its default startup state, the step attenuator is controlled with the clock and reset scheme described above, where each DVGA CLK rising edge changes attenuation by 1/2 step (0.05 dB typical), and the following DVGA CLK falling edge changes attenuation by another 1/2 step (0.05 dB typi-

cal). In other words one complete DVGA CLK cycle changes attenuation by 0.1dB. Alternatively, the Half Step mode may be disabled so that a gain step of 0.1dB will occur on the positive edge of the DVGA CLK and no gain change will occur on the negative edge of the DVGA CLK. The Half Step mode is controlled via SPI™ compatible interface register 0x1Ah, bit 3 (0x1A[3] = “1”, Half Step Disabled, 0.1dB step).

### DVGA CLK Pin

The DVGA clock frequency determines the rate of change of attenuation (i.e. DVGA gain). The DVGA will increment or decrement gain by one step (0.05dB or 0.1dB) with each DVGA CLK cycle when CW/DVGA RST pin is low. The Maximum DVGA clock frequency is 100MHz which sets the maximum gain change rate at 10dB/μs. The minimum DVGA CLK pulse duration (either high or low state) is 4ns. To take advantage of Half Step DVGA clocking, it is recommended to keep DVGA CLK duty cycle close to 50%.

### CW/DVGA RST Pin

When CW/DVGA RST is LOW, the step attenuator will increment or decrement attenuation with each DVGA CLK pulse. In the absence of DVGA CLK, the step attenuator will remain at its current attenuation until either CW/DVGA RST is pulled HIGH or a DVGA CLK pulse is applied. For example, assume DVGA UP is held HIGH while CW/DVGA RST is LOW and 74 clock cycles are applied. The attenuation is reduced by 74 steps or 7.4 dB. If CW/DVGA RST is still held LOW and 10 additional clock pulses are applied, the attenuation is further reduced by 1dB. If CW/DVGA RST is pulled HIGH, the attenuation will return to the DVGA Initial Attenuation (as shown in [Table 4](#)). The first positive CLK edge following a HIGH to LOW DVGA RST transition is valid and will increment or decrement gain depending on whether DVGA UP is HIGH or LOW respectively.

### DVGA UP Pin:

DVGA UP pin determines the DVGA Initial Attenuation point and whether attenuation is decremented or incremented (i.e. DVGA gain increment or decrement respectively). If DVGA UP is HIGH, the DVGA gain will increment upwards, towards the Minimum Attenuation (Maximum Gain) limit of 0dB. If DVGA UP is LOW, the DVGA gain will decrement downwards,

towards the minimum gain limit (38 dB of full attenuation assuming the “attenuation range setting” is at 38dB). DVGA UP can be dynamically switched during an increment or decrement operation.

After DVGA UP is switched from LOW to HIGH (or HIGH to LOW), the first positive edge of DVGA CLK synchronizes the new state with the DVGA CLK. The second positive edge of DVGA CLK will decrement (or increment) the DVGA Gain.

### DVGA Accelerated Gain Adjustment:

With the LM96511's clock and reset scheme and the ability for a high frequency DVGA clock (max = 100MHz), it is possible to get to the desired TGC starting point quickly. Assuming a DVGA “attenuation range setting” of 32dB selected, the fastest way to achieve DVGA attenuations of 16-32 dB is to apply a CW/DVGA RST pulse with DVGA UP HIGH (to get to 32dB attenuation) followed by a succession of DVGA CLK pulses sufficient to get to the attenuation level desired. For attenuations from 0-15.9 dB, it is faster to apply a CW/DVGA RST pulse with DVGA UP LOW (to get to 0dB attenuation) and followed by a succession of fast DVGA CLK pulses. [Figure 21](#) and [Figure 22](#) illustrate examples of this feature in order to explain the accelerated gain adjustment sequence more clearly.

In certain instances, an important parameter may be the time required for this operation (i.e., “T\_attenuation”). Starting from the rising edge of the CW/DVGA RST pulse, the total time is the sum of the CW/DVGA RST minimum pulse width (“T\_RST\_width” = 200ns), the minimum time required to start the DVGA CLK from the CW/DVGA RST's LOW state (i.e., “DVGA RST removal time” which is listed in the Electrical Characteristics Table as, “T\_RST\_rem” = 20 ns), and the time required to clock the DVGA to achieve the desired attenuation (“Attenuation” in dB):

$$T_{\text{attenuation}} = T_{\text{RST\_width}} + T_{\text{RST\_mem}} + 10\text{ns/step} \times (\text{Attenuation} / 0.1\text{dB/step})$$

For  $0 \leq \text{Attenuation} \leq 15.9 \text{ dB}$  (DVGA UP = 0 during clocking)

$$T_{\text{attenuation}} = T_{\text{RST\_width}} + T_{\text{RST\_mem}} + 10\text{ns/step} \times ((32 - \text{Attenuation}) / 0.1\text{dB/step})$$

For  $16 \leq \text{Attenuation} \leq 32 \text{ dB}$  (DVGA UP = 1 during clocking)

For example, with a 32 dB DVGA attenuation range, to achieve 20 dB DVGA attenuation, the time required is:

$$T_{\text{attenuation}} = T_{\text{RST\_width}} + T_{\text{RST\_mem}} + 10\text{ns/step} \times ((32 - \text{Attenuation}) / 0.1 \text{ dB/step})$$

$$T_{\text{attenuation}} = 200 \text{ ns} + 20 \text{ ns} + 10 \text{ ns/step} \times ((32 - 20) / 0.1 \text{ dB/step}) = 1.42 \mu\text{s}$$

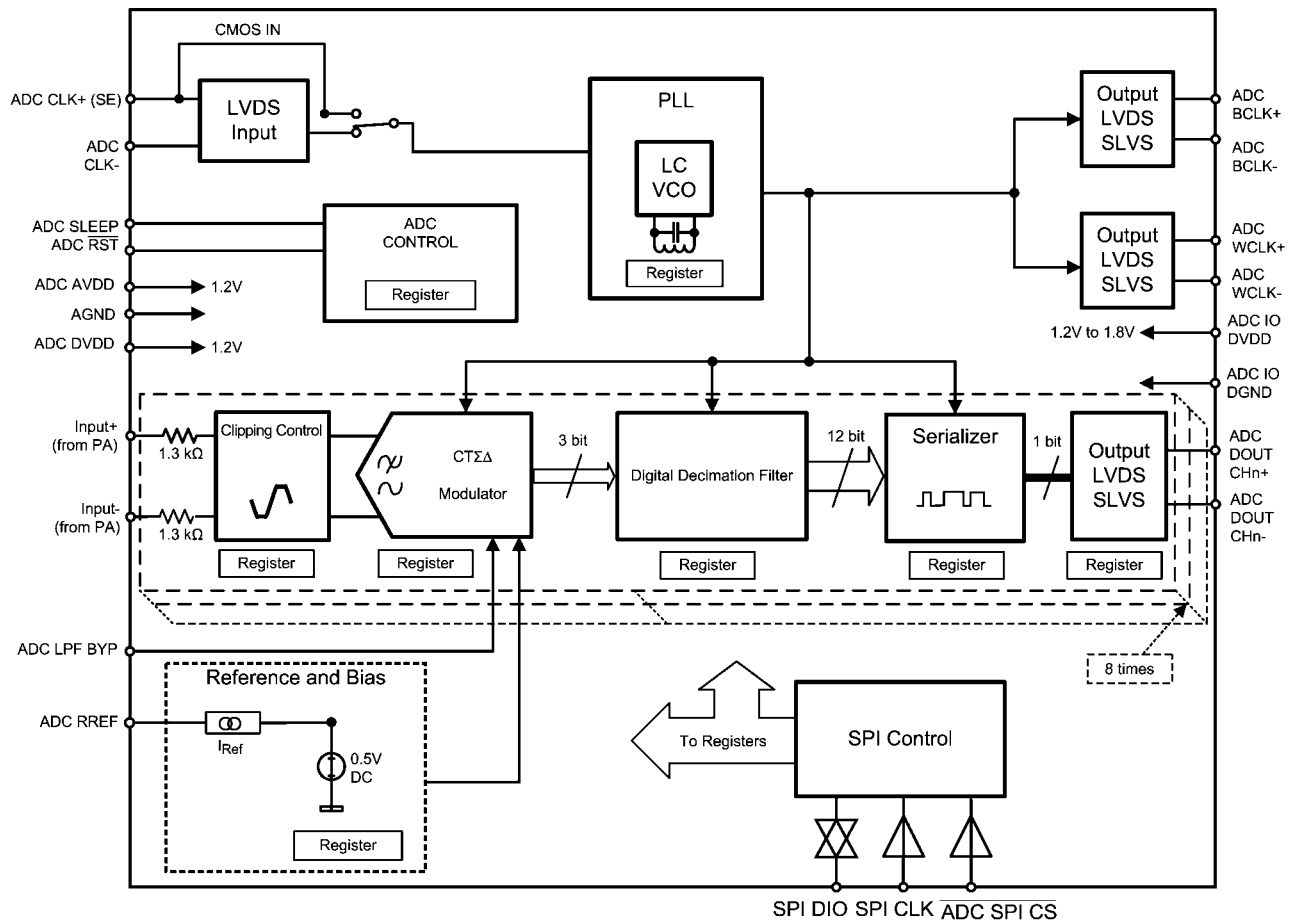
### THE LM96511 ADC

The LM96511 ADC employs a number of unique strategies to provide a high performance multi-channel AFE that offers a significant power consumption reduction when compared to competing architectures, as well as easing system level design. The ultra-low power performance of the LM96511 ADC is derived from the implementation of a fast continuous time sigma delta (CTΣΔ) modulator. Other features of this technology are:

- Intrinsic anti-alias filter: The digital decimating filter provides an intrinsic anti-alias filter, eliminating external

analog filter components, and simplifying multi-channel designs.

- Instant overload recovery (IOR) system guarantees extremely fast recovery from overload (< one clock cycle), and no settling errors on return from overload.
- Ultra-low inter-channel crosstalk.
- Digital Equalizer provides low group delay and hence minimizes signal path delay variation.



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FIGURE 24. LM96511 ADC Block Diagram

The major components of the LM96511 ADC, shown in [Figure 24](#), are: clipping control; CTΣΔ modulator; digital decimation filter; 12-bit serializer; and finally the LVDS/SLVS outputs. The PLL is critical to the operation of the LM96511 ADC, and the PLL also provides the bit and word clock outputs. The SPI™ Compatible Control Interface gives uncomplicated user access to the ADC registers.

#### ADC OUTPUT INTERFACE

The ADC outputs provide a sampling clock and data information. The output sampling or bit clock is a differential high speed bit clock that is 6 times the input clock and 90° out of phase with respect to the output data information. This clock is automatically synchronized to the input ADC clock within the LM96511. However, this bit clock is not phase aligned with the input ADC clock.

The output data information consists of two components: the serialized ADC output data and the output word or frame

clock. Each serialized data word or frame is 12-bits wide. The word clock output provides framing information necessary for deserialization of the data by identifying the bit boundary of each data word sample. The word clock is a lower frequency clock that is phase aligned (within a very small skew,  $t_{DWS}$ ) with the data and is primarily used as a strobe to capture and align data words in a parallel register within the deserializer. The rising edge of the word clock is aligned (within a very small skew) with the LSB of a data word output from the ADC. The word clock signal is sampled on the positive and negative edges of the bit clock output. Thus, a rising edge of the word clock indicates that a full data word is available to load into a deserializer's parallel register and that a new data word begins. This word clock is not phase aligned with the input ADC clock.

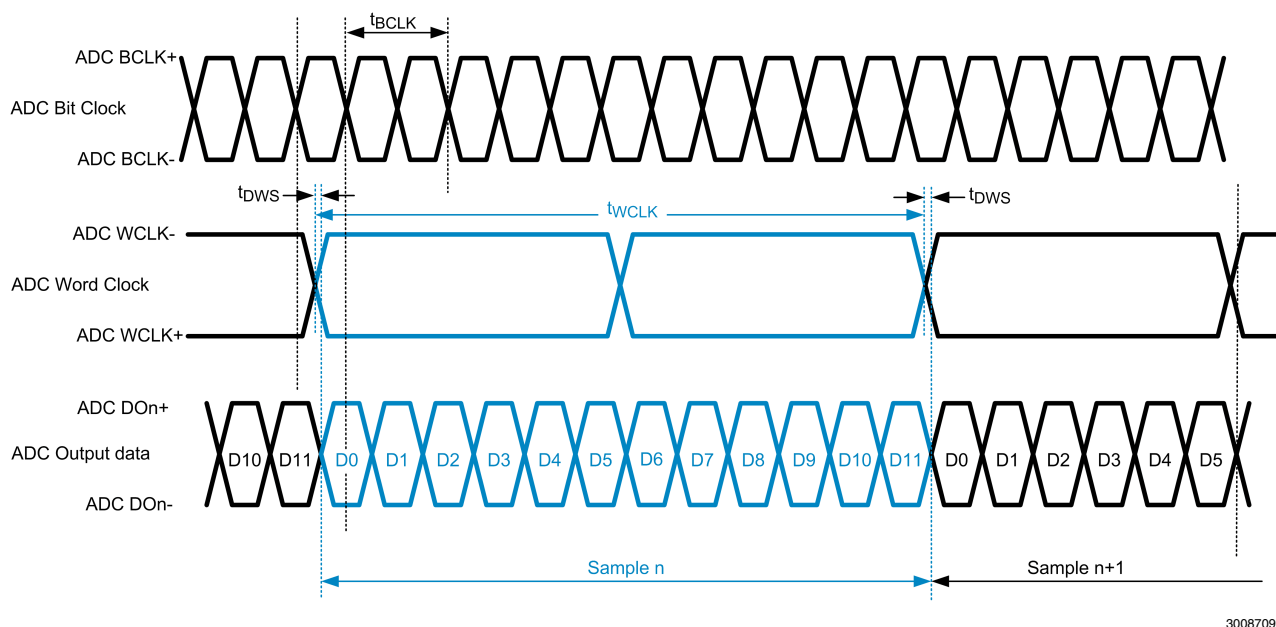


FIGURE 25. ADC WCLK

## 12-BIT SIGMA DELTA ( $\Sigma\Delta$ ) ADC CORE

The LM96511 ADC comprises eight analog ADC channels using a CT $\Sigma\Delta$  architecture, which provides very high dynamic performance with ultra-low power, while operating from a minimal 1.2V supply.

The CT $\Sigma\Delta$  ADC architecture uses a third order sigma delta modulator operating at a nominal 16 times over-sampling rate in combination with a 3-bit quantizer. The modulator output is coupled to a power efficient digital decimation filter that decimates the high rate modulator output (640 to 800 MHz) to provide output data at a sample rate between 40 MSPS and 50 MSPS. A benefit of the CT $\Sigma\Delta$  design is that the ADC requires no external anti-alias filters for most applications. This benefit is derived from a combination of the design of the analog sigma delta modulator and digital decimation filter. The digital filter achieves a steep transition band, and provides 72 dB of attenuation in the stop band. Using the digital equalizer, the signal transfer characteristics including phase performance can be optimized so as to minimize group delay variation. In applications where it is not required, the digital equalizer can be disabled to further save power.

## INSTANT OVERLOAD RECOVERY

The LM96511 features an overload handling system which provides instantaneous recovery from signals driving the ADC inputs beyond the full-scale input range. The ADC can operate in two different modes. In the default ADC mode (IOR Off mode) a full-scale input range of  $4.2 V_{PP}$  is supported, here the ADC operates with some inherent overload recovery time, similar to a conventional ADC.

In the IOR On mode, the ADC has a reduced  $3.2 V_{PP}$  full scale input range, but provides a significant benefit in that the ADC can now be driven by input voltages as high as 5 dB beyond the nominal full-scale ( $f_{IN} < 12$  MHz), that is  $5.7 V_{PP}$ , and will recover instantaneously. In a number of applications this feature can help simplify input stage design and manufacturing set-up and calibration. The LM96511 recovers immediately from overload with no missing codes and no settling time.

The proprietary strategy used within the LM96511 ADC uses high speed patented clamp techniques to limit the input signal and keep it within the stable input range of the ADC. This process happens at a speed equivalent to the on-chip over-sampling rate of 640 to 800 MHz. The advantage of this system is that it responds immediately to out of range signals. While the inputs are over-range the ADC outputs a full scale result. As the over-range input is removed the ADC adjusts to the input signal level and is able to provide sampled data instantaneously. The LM96511's behavior on emerging from overload is repeatable and independent of whether the input signal was positive or negative going at the point of overload.

## USING IOR ON MODE

As discussed earlier, IOR On mode provides instantaneous recovery from overload conditions, with no ringing and correct data output as soon as the input returns in range.

### Standard Use of IOR On Mode

The recommended way to enable IOR On mode is by setting bit 4 (IOR) of the Modulator Overload Control register (02h). Setting this bit will enable IOR mode with the default settings for Digital Gain Factor (DGF) in the Decimator Clipping Control register (0Ah) and OL in the Modulator Overload Control register (02h). Setting the IOR mode bit to 0 will restore DGF and OL to their default values, hence putting the LM96511 back into IOR Off mode.

As can be seen in the Electrical Specifications, using IOR On mode gives a slight reduction in SNR performance, and also a reduction of the full scale input range to  $3.2V_{PP}$  differential.

### Advanced Use of IOR On Mode

The registers described above allow the user to customize IOR On mode. In order to correctly set the DGF and OL values, it is necessary to understand how the IOR On mode functions. The implementation of IOR On mode in the LM96511's ADC consists of analog and digital parts working in tandem.

The analog clipping circuitry, controlled by OL, is designed to protect the sigma delta modulator from large signal inputs. Using an analog clamp, signals are soft-limited to the less than the  $4.2V_{PP}$  full scale range of the modulator. OL gives the value at which the circuit will begin to clamp.

The digital filter of the ADC12EU050 is where the full scale input range is selected and the hard limiting of the signal takes place. DGF selects the gain of the digital filter, and hence the new full scale input range of the ADC.

In order to set a custom value for DGF, Custom Gain Setting (CGS), bit 7 of the Decimator Clipping Control register (0Ah), must be set. The DGF can then be set, based on the application requirements. OL should then be set to a value approximately half-way between the new full scale input range (which was just selected by DGF) and the default full scale input range of  $4.2V_{PP}$ . OL must be set to a value higher than DGF, otherwise the signal will be limited by the analog clipping circuitry, rather than the digital circuitry, and overload recovery will be impacted.

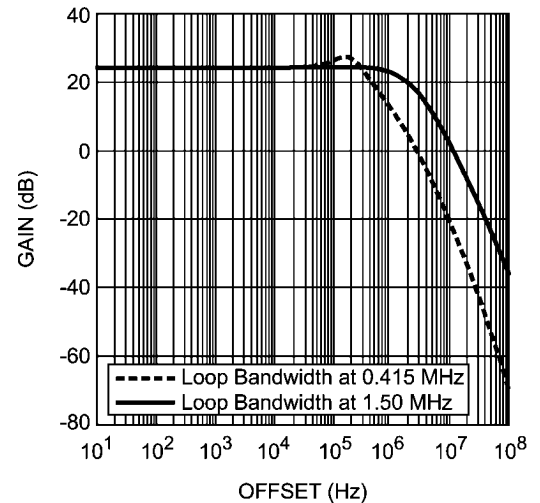
### INTEGRATED PRECISION LC PLL ADVANTAGES

The LM96511 ADC includes an integrated high performance “clean up” phase locked loop (PLL), simplifying the need for a low jitter external clock for ADC CLK pin(s). The PLL serves three important functions; it generates a highly accurate internal sampling clock source of up to 800 MHz; a clock for the LVDS serializers at 600 MHz; and it provides a low jitter clock for other internal components. With its jitter clean-up capability this PLL allows lower performance system clocks to be used.

The ADC CLK pin(s) are AC coupled within the LM96511 so that the common mode voltage is not critical. The clock can be single ended or differential (unused ADC CLK input can be grounded). A single ended clock input should be connected to ADC CLK+ (B22) pin, and ADC CLK- (A22) pin should be grounded. Furthermore, the ADC CLK source can be a sine or square wave for maximum flexibility. Datasheet parameter testing is done with a “clean”, differential square wave clock source routed as  $100\Omega$  differential pairs, and terminated with a  $100\Omega$  resistor close to LM96511 clock inputs.

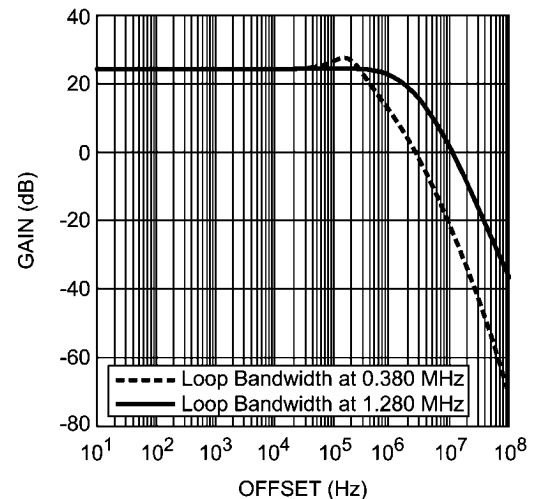
The benefit of having an on chip PLL is that in most applications a high precision clock source is not required. The impact of aperture jitter on the ADC's performance is reduced dramatically by the jitter clean-up properties of the PLL, which ensures that any RMS jitter outside of the PLL bandwidth is attenuated. The PLL also significantly relaxes the input clock duty cycle requirements, accepting input clock duty cycles of 20% to 80%.

The PLL offers two choices of bandwidth, selectable by SPI™ register 03h[1] (SHBW). For the majority of systems, the default bandwidth of 415 KHz is suitable. If the system already contains a high performance clock, with excellent RMS jitter performance up to a 1.5 MHz bandwidth, then the PLL's high bandwidth mode may be used.



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FIGURE 26. PLL Phase Noise Transfer Function: ADC CLK = 40 MHz



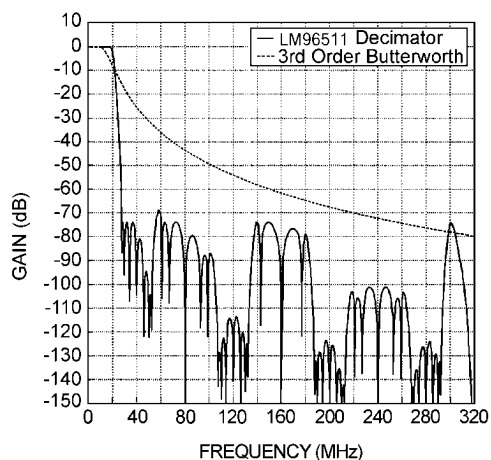
30087042

FIGURE 27. PLL Phase Noise Transfer Function: ADC CLK = 50 MHz

On the input clock, excessive RMS jitter within the PLL bandwidth will be seen in the output spectrum as sidebands, or close in phase noise, around the fundamental signal.

### DIGITAL DECIMATION FILTER AND EQUALIZER

The digital decimation filter is an integral part of the sigma delta architecture. It decimates the over-sampled data from the modulator down to the sample rate, and its extremely sharp low pass characteristic combined with the modulator's broad band response provides the intrinsic anti-alias filter. The digital low pass filter exhibits 72 dB of attenuation in the stop band. Figure 28 shows the digital filter transfer function at 40 MSPS, compared to a third order Butterworth transfer function.

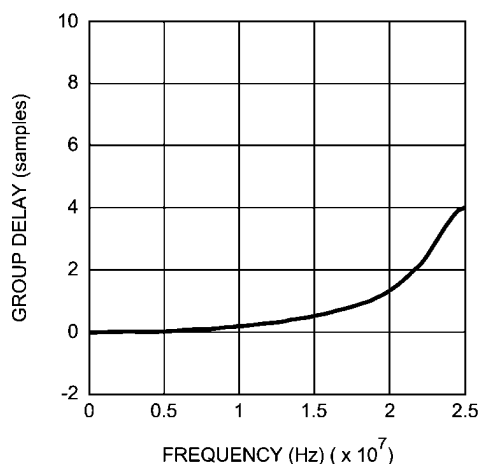


30087043

FIGURE 28. Digital Filter Transfer Function

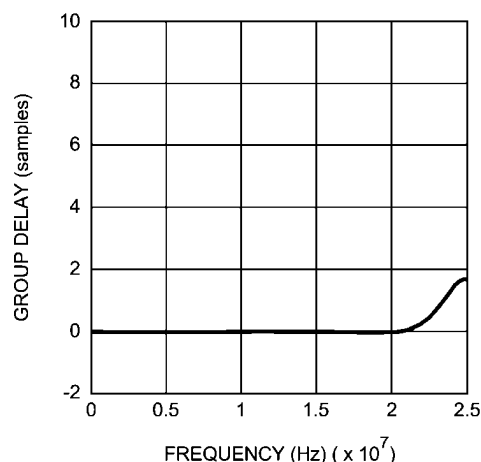
Due to the digital implementation of the filter, the filter parameters automatically scale with the ADC sampling frequency. Such steep digital filters introduce group delay problems, but the LM96511 ADC includes a digital equalizer, which reduces group delay ripple variation to less than 0.05 samples. In applications where group delay is not of concern, the equalizer can be turned off through the SPI™ interface (register address 0Bh) in order to save power.

Figure 29 and Figure 30 show the group delay ripple of the digital decimation filter at 50 MSPS, firstly with the equalizer disabled, and secondly with the equalizer enabled:



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FIGURE 29. Group Delay with Equalizer Off



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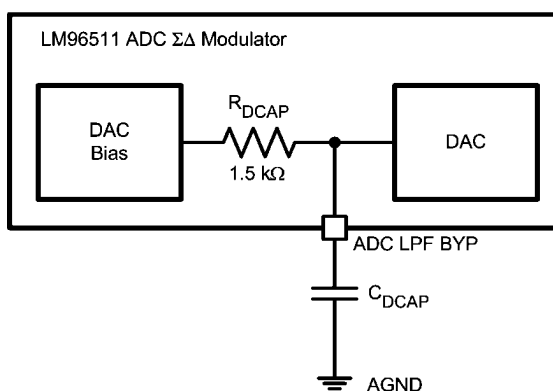
FIGURE 30. Group Delay with Equalizer On

### OUTPUT CLOCK SYNCHRONIZATION ACROSS MULTIPLE CHIPS

In systems containing more than one LM96511, it is often required that the timing of output samples is synchronized across the multiple chips. The PLL in the LM96511 ADC takes care of this automatically by frequency-locking the output clocks with the input clock for each LM96511 device. However, the user must still ensure, using correct board layout and clock buffering techniques, that the input clock to each LM96511 ADC (ADC CLK) is synchronized to each other. If this is the case, then the output bit clocks from each LM96511 ADC will also be synchronized. This means that output samples are aligned with each other.

### CAPACITOR SELECTION

The ADC LPF BYP pin provides the capacitance for the low pass filter between the DAC bias block and the DAC in the sigma-delta modulator. The filter blocks noise from the DAC Bias block from entering the DAC. Any noise which passes through this filter will be seen in the spectrum as side skirts around the carrier. The filter circuit, which is a first order RC filter, is shown in Figure 31



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FIGURE 31. DAC LPF Capacitor

The ADC LPF BYP pin must be connected to AGND through a low leakage, minimum 100 nF capacitor. If the application is especially sensitive to close to the carrier phase noise, then it is recommended to increase  $C_{DCAP}$ , up to a maximum of 10  $\mu$ F. For other applications where close to the carrier phase noise is not important, the capacitor can be kept small in order to reduce costs and minimize board space. The corner frequency of this filter is determined by the equation:

$$f = \frac{1}{2\pi R_{DCAP} C_{DCAP}}$$

## ADC OUTPUT CONSIDERATIONS

The LM96511 offers a variety of output settings in order to cater for different system design and integration needs

### Output Driving Voltage, ADC IO DVDD

The ADC output driver voltage, ADC IO DVDD, can be set between 1.2V and 1.8V. An ADC IO DVDD of 1.2V will offer the lowest power consumption. Because ADC IO DVDD can be varied, the LM96511 provides, via the SPI™ registers, the ability to adjust the output common mode voltage.

### Output Modes and Output Common Mode

Three different output modes are also supported: SLVS, LVDS and reduced common mode LVDS. SLVS and LVDS modes output data according to their respective specifications. Reduced common mode LVDS must be used when the output driver voltage, ADC IO DVDD, is 1.2V. The standard LVDS common mode voltage is 1.2V, which is obviously not feasible if ADC IO DVDD is 1.2V. Therefore, the output common mode voltage must be set to 1.0V by setting the bit OCM in the LVDS Control Register to 0.

When ADC IO DVDD is 1.8V, the standard LVDS common mode voltage of 1.25V must be used, by setting OCM (SPI™ Register 0Ch) equal to 1. Table 2 summarizes these different output modes:

TABLE 1. ADC Output Mode Summary

| Output Mode     | ADC IO DVDD (V) | SPI™ Register 0Ch[1] (OCM) | SPI™ Register 0Ch[0] (SLVS) | Output Common Mode (V) |
|-----------------|-----------------|----------------------------|-----------------------------|------------------------|
| Reduced CM LVDS | 1.2             | 0                          | 0                           | 1.0                    |
| LVDS            | 1.8             | 1                          | 0                           | 1.25                   |
| SLVS            | 1.2             | X                          | 1                           | 0.175                  |

SLVS mode offers the lowest power consumption followed by reduced common mode LVDS and then the standard LVDS. As well as the different output modes, the output drive current can also be controlled via the LVDS Control Register. The default output drive current is 2.5 mA, but this can be increased to 3.5 mA or 5 mA, depending on output trace routing and receiver requirements. Power consumption of the LM96511 will increase slightly as the output driver current is increased.

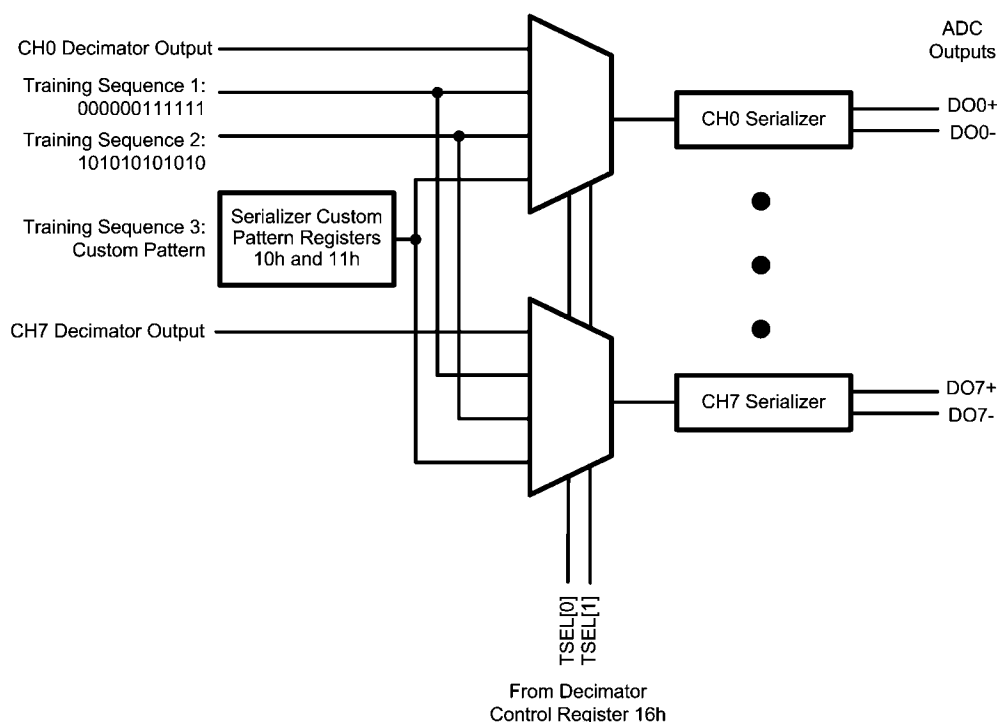
### Termination

The final control feature available in the LVDS Control Register is the choice between internal and external 100 $\Omega$  termination. Although the termination is recommended to be as close to the receiver as possible, in some cases it may be necessary or desirable to perform this termination at the transmitter. Internal 100 $\Omega$  termination at the transmitter (the LM96511) is enabled by setting the SPI™ register bit TX\_term to 1.

### LVDS Output Training Sequences

Often it is necessary to calibrate the LVDS receiver, for example an FPGA or DSP, so that skew between the eight ADC output channels is minimized. In order to simplify this process, the LM96511 provides three LVDS training modes, where a pre-defined or custom pattern is output on all eight channels simultaneously. While a training mode is active, the word and bit clocks are output as usual. In order to select a training mode, the TSEL bits of the Decimator Control Register (0Bh) must be programmed via the SPI™ compatible interface.

There are two pre-defined training patterns, or a custom pattern can be loaded via the SPI™ compatible interface into the Serializer Custom Pattern 0 and 1 Registers (08h and 09h). In order to return to normal ADC operation after skew calibration, the TSEL bits should be returned to their default value of 00.



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FIGURE 32. LVDS Training Sequence

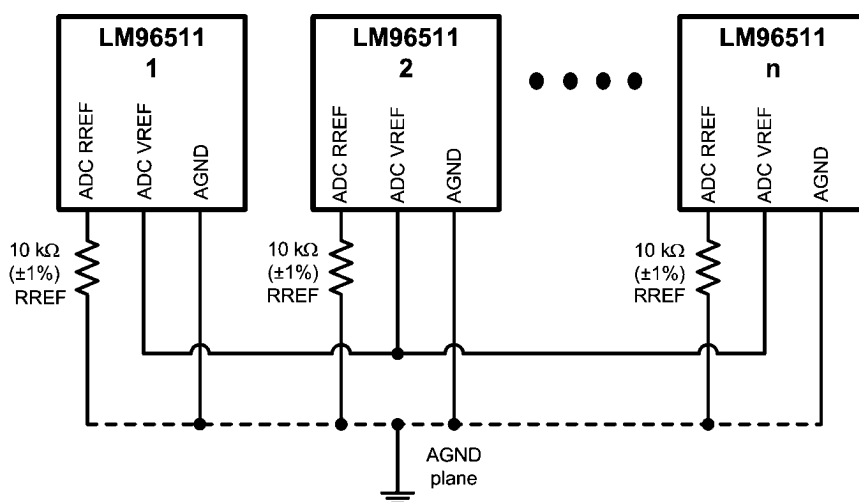
## The Voltage Reference

The LM96511 ADC provides an on chip,  $\pm 5\%$  tolerance voltage reference (ADC RREF), together with all necessary biasing circuits and current sources. A  $10\text{k}\Omega$  ( $\pm 1\%$ ) resistor (RREF) must be connected between ADC RREF and AGND in order to establish the biasing current of the ADC.

If a tighter tolerance reference is required for improved thermal stability, an external voltage reference can be connected between the ADC VREF and AGND pins. This external ref-

erence must be able to support a  $20\text{k}\Omega$  internal load tied to the internal voltage reference (500 mV nominal). The RREF resistor must be connected even when using an external reference.

When using the internal reference, ADC VREF should be connected to AGND through a  $100\text{ nF}$  capacitor. Chip-to-chip gain matching between several LM96511 ADCs can be improved by connecting the ADC VREF pins of the ADCs. This is shown in [Figure 33](#):



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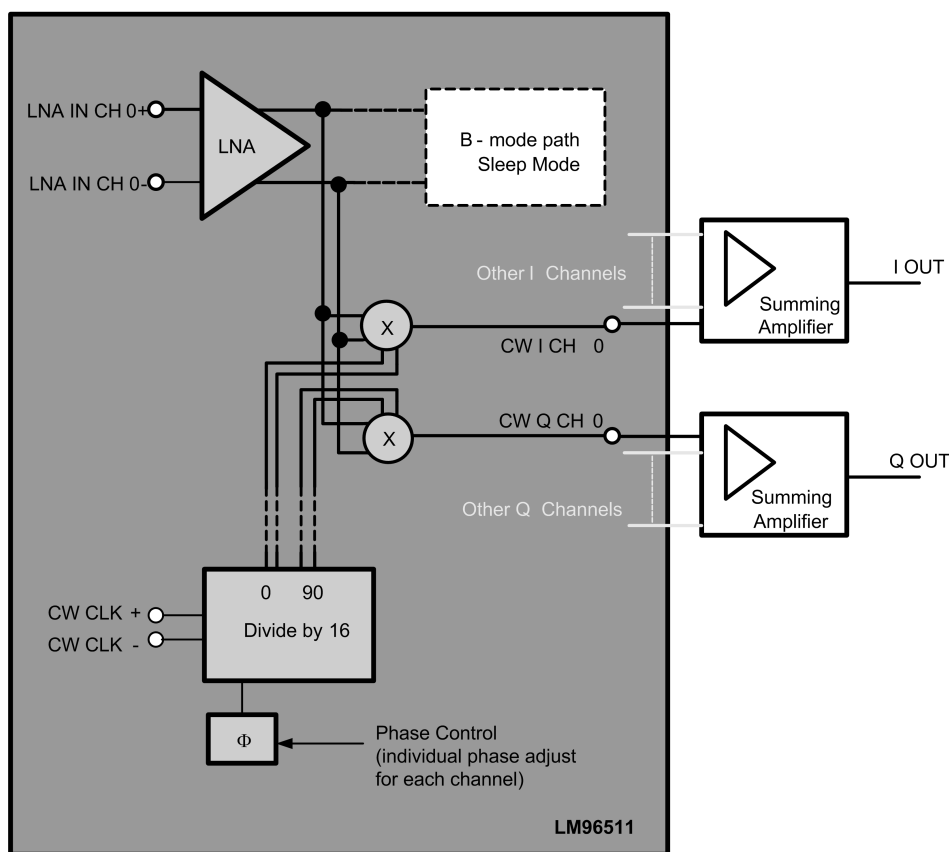
FIGURE 33. Reference Sharing

## CW Doppler Section Theory of Operation

As illustrated in [Figure 34](#) below, the LM96511 includes a CW Doppler demodulator for analog beamforming in ultrasound applications. Eight single-ended in-phase (CW I Chx) and quadrature (CW Q Chx) output pin currents (16 total pins for 8 channels) are summed together using an external summing amplifier (one each for I and Q outputs) as shown. Each channel's phase can be controlled in  $22.5^\circ$  increments using a 4 bit phase code with an SPI™ compatible interface register. With a common RF input applied to all channels and the same phase code programmed, all 8 channels' outputs will be nominally in phase (I to I and Q to Q). If, for example, Channel 5's phase code is changed from the default value of 0000 to 0101, the Channel 5 output will lead any Channel with phase code 0000 by  $112.5^\circ (= 5 \times 22.5^\circ)$ . With N-phase-aligned channels summed together, the SNR increases by  $\sqrt{N}$  or 3 dB every

time N doubles, since the CW Doppler signal increases by N but uncorrelated noise increases by  $\sqrt{N}$ . Similarly, the LNAs and demodulators do not share any references or internal functions in order to keep their noise contributions uncorrelated.

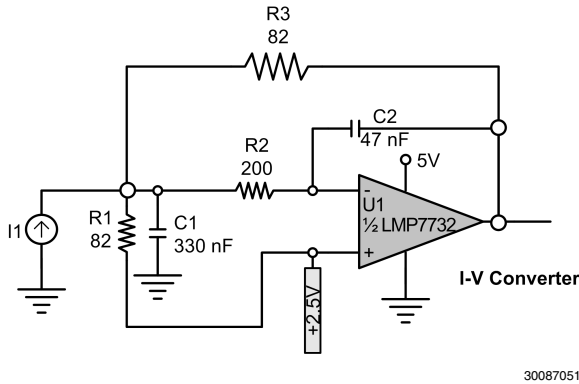
The CW Doppler section requires a differential 16x Local Oscillator (LO) input (CW CLK inputs in ). The clock source used must have high fidelity and low phase noise to maintain low Doppler phase noise. The typical LO common mode (CM) level is 1.2V with a 0.4Vpp differential swing ( $100\Omega$  differential source). Internally, the LO input is divided by 16 and fed to doubly-balanced demodulators. The LO duty cycle should be close to 50%. A Doppler Reset pin is provided (CW/DVGA RST) which resets all the LO dividers to allow synchronization by placing the divider's individual counters in a known state. This allows several LM96511's to be used with additional channels.



30087050

**FIGURE 34. Signal Path (CW Doppler) Single Channel**

Individual I and individual Q outputs are summed together using a single-supply summing amplifier which observes the LM96511 Doppler output compliance range (2.1V to 3.6V). [Figure 35](#) shows one such implementation employed on the LM96511 Reference Board (available for purchase from National Semiconductor):



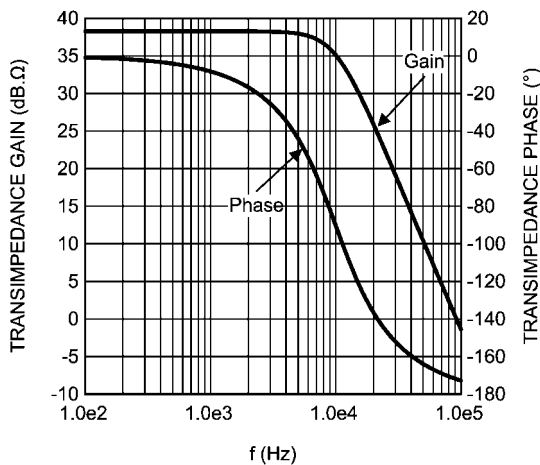
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FIGURE 35. I-V with Integrated 2-Pole LFP

It is important to be mindful of noise, especially 1/f noise in the power supplies, particularly the “+2.5V” supply tied to the non-inverting input of the summing Op Amp.

A low noise Op Amp (LMP7732) is selected for this application to minimize the noise impact. The “I1” current source represents a single output current from the CW Doppler section of the LM96511. Other outputs can be paralleled together. The I-V converter output is then AC coupled to a 24-bit ADC (Asahi-Kasei (AKM) Part # AK5386VT) input for acquisition and processing. The use of a high bit count (or pro-audio grade) ADC is essential in keeping the noise floor low to maximize SNR.

The I-V converter of Figure 35 is biased for single supply ( $V_{CC}=5V$ ) operation with its non-inverting input tied to a low noise +2.5V reference. The Feedback action ensures low CW DOPPLER output compliance. The 2<sup>nd</sup> order Butterworth LPF in Figure 35 has a passband gain of  $\sim 38 \text{ dB}/\Omega$  ( $=R3=82 \text{ V/Amp}$ ). Figure 36 shows the I-V converter's transfer function:



30087052

FIGURE 36. CW Doppler LPF Gain/Phase Characteristics

With a typical  $\pm 4.2 \text{ mA}$  from each CW DOPPLER output and 4 channels summed together, the Op Amp output voltage is  $\pm 1.38V$  ( $= \pm 4.2 \text{ mA} \times 4 \times 82 \text{ ohm}$ ) from  $V_{CC}/2$ , which can be supported with a single 5V supply and the op amp's Rail-to-Rail output. The LMP7732 has approximately  $17 \text{ mA}$  ( $\pm 4.2 \text{ mA} \times 4$ ) output current capability required when its output is at least 0.4V away from either rail, which is the present case.

The LPF in Figure 35 has a -3dB bandwidth of 10 KHz, suitable for CW Doppler blood flow applications. The Doppler shift expression below shows the shift in frequency as a function of target speed:

$$\Delta f_D = \pm \frac{2\Delta v}{\lambda} \cos \theta$$

where:

- $\Delta f_D$  = Change in frequency (CW Doppler output tone frequency) (Hz)
- $\Delta v$  = Speed difference between target and ultra source (m/s)
- $\lambda$  = Wavelength of ultra-sound signal (m/cycle)
- $\theta$  = Angle between incident wave and the velocity vector of the moving target

With a typical ultrasound propagation speed of 1540 m/s and 5MHz repetition rate, the wavelength,  $\lambda$ , is 308  $\mu\text{m}/\text{cycle}$ . Assuming a  $0^\circ$  incidence angle, blood flowing at around 15 cm/s will produce a frequency shift of 974 Hz:

$$\frac{2 \times 0.15(\text{m/s})}{308(\mu\text{m/s})} \times \cos(0)$$

#### CW DOPPLER NOISE ANALYSIS

The combination I-V converter & LPF of Figure 35, slightly degrades the LM96511 Doppler output noise. From the CW Doppler Electrical Characteristics Table, with 53 pA/ $\sqrt{\text{Hz}}$  typical RMS noise from each of the four LM96511 outputs summed, one can expect 8.7 nV/ $\sqrt{\text{Hz}}$  ( $= 53 \text{ pA}/\sqrt{\text{Hz}} \times 82\Omega \times \sqrt{4}$ ) of typical RMS noise voltage density at the I-V converter output, assuming a noiseless I-V converter.

The I-V converter noise contribution is dominated by the LMP7732's voltage noise ( $= 2.9\text{nV}/\sqrt{\text{Hz}}$ ) and its noise gain ( $\approx (1+R3/R1) = 2V/V$  passband approximation) resulting in 5.8nV/ $\sqrt{\text{Hz}}$  typical rms noise at the output. Resistor (R1-R3) thermal noise accounts for another 3.9nV/ $\sqrt{\text{Hz}}$  for a total RSS noise of 7nV/ $\sqrt{\text{Hz}}$  at the I-V converter output. The impact on the LM96511 related noise is 2.3 dB :

$$20 \times \log \frac{\sqrt{(7.0 \text{ nV}/\sqrt{\text{Hz}})^2 + (8.7 \text{ nV}/\sqrt{\text{Hz}})^2}}{8.7 \text{ nV}/\sqrt{\text{Hz}}}$$

With a 10 kHz LPF and the LM96511's typical  $\pm 3\text{mA}$  current from each output, and assuming a sinusoidal peak-to-RMS ratio of  $\sqrt{2}$ , one can expect a SNR of 119 dB:

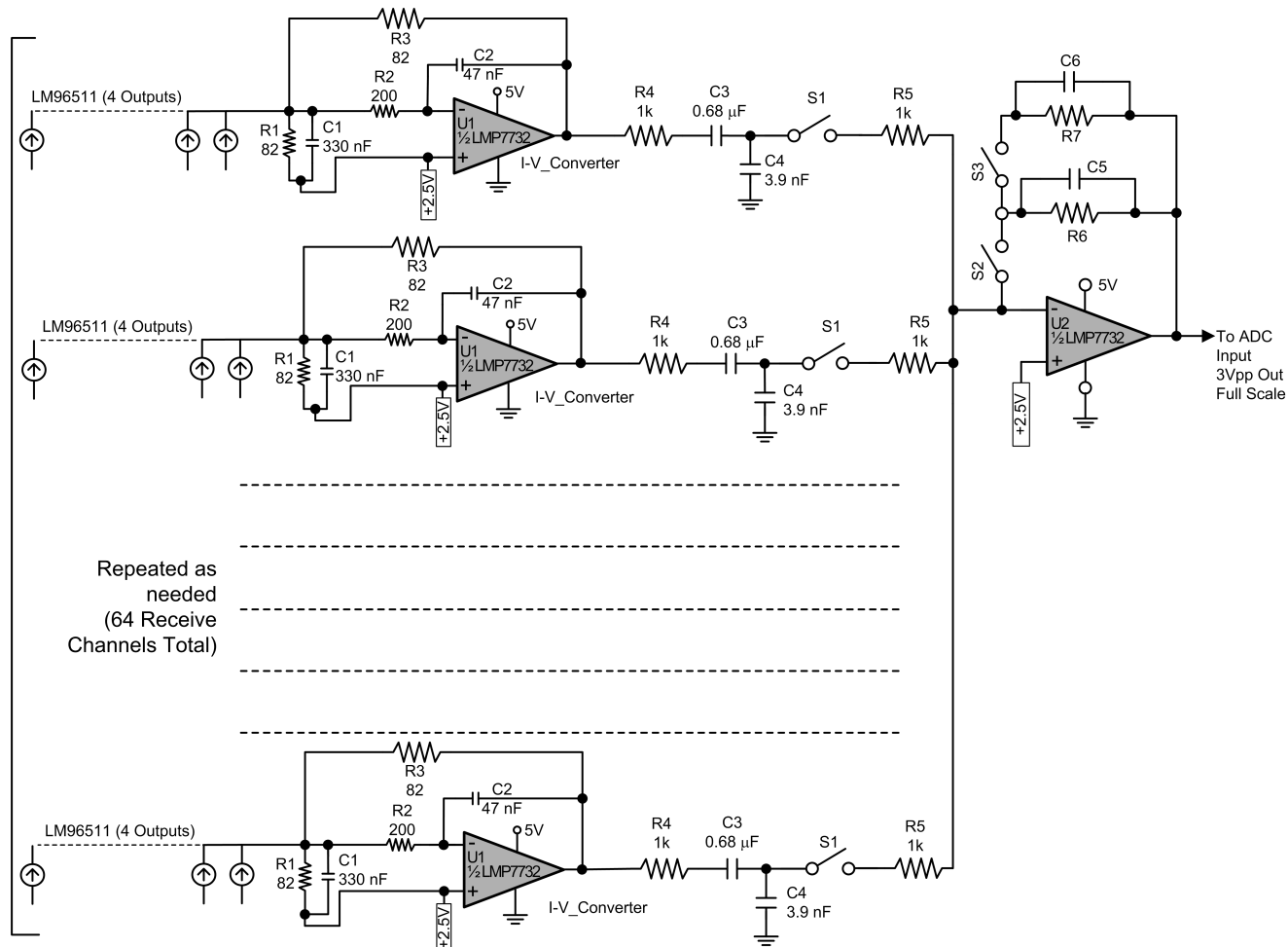
$$20 \times \log \frac{3 \text{ mA} \times 8 \times 82\Omega \times 1/\sqrt{2}}{\sqrt{(7 \text{ nV})^2 + (8.7 \text{ nV})^2} \times \sqrt{10 \text{ kHz}}}$$

Note that the LMP7732's low 1/f noise corner frequency ( $= 3\text{Hz}$ ) helps in keeping the 1/f noise inconsequential thus maintaining high SNR.

Figure 37 shows an implementation of 64 CW Doppler receive channels for either “I” or “Q” outputs. Each LM96511 CW Doppler output is represented by a current source symbol. In this implementation, each primary I-V converter (U1) handles 4 channels while U2 sums the outputs of all I-V converters. R4, R5, C3, and C4 form a combination high-pass and low-pass filter that strips the DC component and attenuates the

signals beyond ~50 KHz. Analog switch S1 is used to selectively shutdown channels; Often, a 128 channel ultrasound system operates with 64 receive channels. Switches S2 and S3 are used to set the overall gain. This is commonly done to optimize dynamic range depending on the target Doppler

echo. The U2 gain is set for FS output ( $3V_{pp}$  in this case) with offset frequency signal amplitudes typically 20 dB down from the FS CW Doppler output, or about  $\pm 0.42$  mA from each LM96511 output.



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FIGURE 37. CW Doppler Output (I or Q) Implementation (64 Receive Channels)

#### CW DOPPLER 16x LO SOURCE IMPLEMENTATION

In order to achieve the phase noise performance specified in the Electrical Characteristic table, the CW\_Doppler 16x LO source (CW CLK input pins) should have low jitter (low phase noise). The performance specifications reflected in this datasheet were obtained with highly accurate 80 MHz (for 5MHz CW\_Doppler signal) sources made by Wenzel Associates, Inc. Their oscillators exhibit ~ -165 dBc/Hz @ 10 KHz phase noise. The 16xLO implemented in the LM96511 Ref-

erence design, uses a lower cost oscillator from Vectron International, which exhibits acceptable phase noise performance (-145 dBc/Hz @ 10 KHz) in conjunction with National Semiconductor's LMK01000 low phase-noise clock buffer-divider chip. By dividing down from a higher frequency source, one can achieve 6dB of improvement in phase noise for every divide-by-two. The block diagram below shows this in more detail:

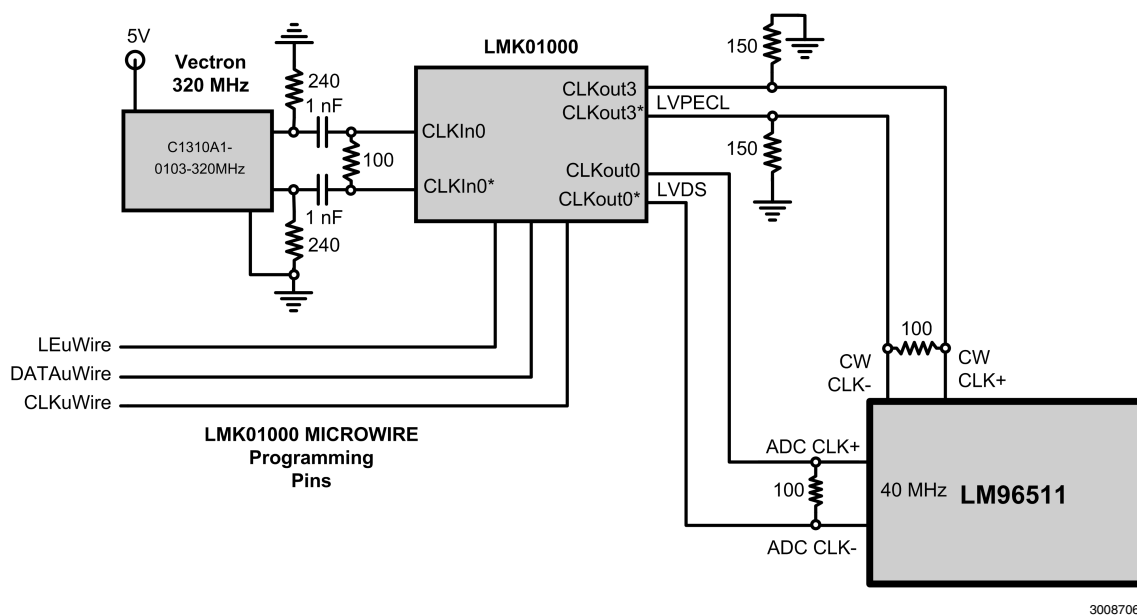


**FIGURE 38. CW Doppler Low-Phase Noise Clock Source Design**

In [Figure 38](#), a low phase noise 320 MHz source is divided by 4 (MICROWIRE programmable) in an LMK01000 to provide an 80.0 MHz CW CLK for a 5.0 MHz ultrasound signal. Other LMK01000 outputs are available for auxiliary functions like the 40 MHz B-mode ADC clock. Keep in mind however that

the low-phase noise of this approach is not required by the B-mode ADC CLK because of its integrated PLL.

The faster edges and lower signal swing of the LMK01000's LVPECL outputs (CLKout3-7) provide better phase noise performance (lower jitter) than the LVDS outputs (CLKout0-2).

## LM96511 Power Management

TABLE 2. LM96511 Power Consumption for Various Conditions

| AMP CW/<br>DVGA & ADC<br>CW/DVGA<br>Pins | Operating<br>Condition | LNA                                   | DVGA                                   | Doppler<br>Demod. | ADC                  | Total Power<br>Consumption |
|------------------------------------------|------------------------|---------------------------------------|----------------------------------------|-------------------|----------------------|----------------------------|
| 0                                        | B-Mode                 | ON<br>(LNA PD=LO)<br>280 mW           | ON (DVGA<br>PD=LO)<br>230 mW           | OFF<br>24 mW      | ON<br>350 mW         | 884 mW                     |
|                                          | —                      | POWER<br>DOWN<br>(LNA PD=HI)<br>12 mW | POWER<br>DOWN<br>(DVGA PD=HI)<br>14 mW |                   | SLEEP MODE*<br>40 mW | N/A                        |
| 1                                        | CW Doppler Mode        | ON (LNA<br>PD=LO)<br>280 mW           | POWER<br>DOWN<br>14mW                  | ON<br>1.3W        | 40 mW                | 1.63W                      |
|                                          | —                      | POWER<br>DOWN<br>(LNA PD=HI)<br>12 mW |                                        |                   |                      | N/A                        |

\* ADC in Sleep Mode using SPI™ compatible register 00h[1]. See SPI™ compatible Register Map.

The ADC within the LM96511 operates normally at ultra-low power levels. In addition, several power management modes are provided:

- Power Down (Accessible through PD bit of Top Control Register, 00h[0], or through individual channel power down, 01h[0-7]. See SPI™ compatible Register Map)
- Sleep (Accessible through SLEEP bit of Top Control Register 00h[1]. See SPI™ compatible Register Map)

Power Down is the lowest power consumption mode, but with a longer wake-up time than Sleep mode. In power down mode, all circuits in the ADC chip are turned off, including the PLL, reference and bias circuits.

The LM96511 ADC Power consumption in Sleep mode is higher than in Power Down mode, but pin access (ADC CW/DVGA pin) and fast wake-up enables duty cycle powering of the ADC.

The LM96511 ADC also allows channel by channel Power Down through the ADC/ LVDS Channel Power Down register (SPI™ register 01h[0-7]). When a single channel is in Power Down, the  $\Sigma\Delta$  modulator, digital decimating filter and LVDS outputs for that channel will be shut off, with the corresponding single channel reduction in power consumption.

### POWER-UP SEQUENCING

The ADC within the LM96511 should be powered-up prior to the amplifier section. The ADC contains a power-on reset circuit,

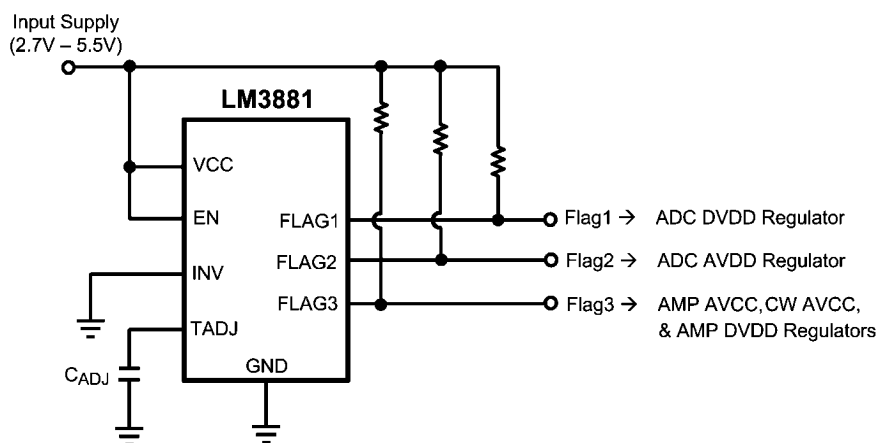
connected to ADC AVDD. To ensure correct reset operation, the power supplies should be provided in the following order (10 ms minimum delay between each supply):

1. ADC IO DVDD (connected to AMP IO DVDD) (1.2V)
2. ADC DVDD (1.2V)
3. ADC AVDD (1.2V)
4. The remaining supplies simultaneously or in any order: AMP AVCC A (3.3V), CW AVCC (5V), AMP DVDD (3.3V)

Additionally, it is required that the rise time for ADC DVDD and ADC AVDD each is longer than 40  $\mu$ s.

If the ADC power-up sequence order above (steps 1-3) is not followed, then , prior to amplifier power-up (step 4), the user should apply a 10ms duration reset via the reset pin ( $\overline{ADC\ RST}$ ), and wait another 10ms before applying the amplifier power (step 4).

One method of power sequencing is to use the LM3881, or equivalent, Power Sequencer IC. When used with on-board regulators with shutdown capability (e.g. LP3878), the LM3881 can provide a simple, cost-effective way of controlling the sequence of 3 supplies.



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**FIGURE 39. LM3881 Power Sequencer Can be Used for Proper LM96511 Power-Up**

LM3881's "Flag1" output is the first to come-up and "Flag3" is the last. For the LM96511, the ADC IO DVDD regulator will be the first to come-up and thus need not be controlled by the LM3881. ADC DVDD will be controlled by the LM3881 "Flag1"

output, ADC AVDD by "Flag2" output, and "Flag3" powers-up the rest of the supplies simultaneously.

To power down, turn off the voltages in the exact reverse order.

#### Recommended Operating Conditions

|                                        |                                                   |
|----------------------------------------|---------------------------------------------------|
| IOR                                    | On (SPI™ Register 02h[4]= 1)                      |
| ADC Sampling Rate                      | 40/45 MSPS (SPI™ Register 00h[4]=1)               |
| DVGA Initial Attenuation (See Table 5) | 32dB (DVGA INIT MSB = HI, DVGA INIT LSB = HI)     |
| DVGA PA HI                             | LO                                                |
| ADC Data Out                           | LVDS                                              |
| Equalizer                              | Off (SPI™ Register 0Bh[4]=0) (Default)            |
| CGS                                    | Auto Gain (SPI™ Register 0Ah[7]= 0) (Default)     |
| SHBW (PLL Bandwidth)                   | Low Bandwidth (SPI™ Register 03h[1]= 0) (Default) |
| DVGA Half-Step Disable                 | 0 (SPI™ Register 1Ah[3]= 0) (Default)             |
| All Other Conditions                   | Default                                           |

## SPI™ Interface

### THE SERIAL PERIPHERAL INTERFACE

The LM96511 provides several user controlled functions which are accessed through a standard SPI™ compatible, Serial Interface. Figure 40 illustrates a method to convert a “four wire” SPI™ compatible controller (Data Out, Data

In, Clock, and Chip Select) to the “three-wire” (bi-directional Data In / Out) SPI™ compatible interface required by LM96511. The Serial Interface offers users with a range of supply voltages from 1.2V to 1.8V. The Level Translator shown allows the SPI™ Controller to Write to or Read from the LM96511 even if it uses a different supply voltage than LM96511.

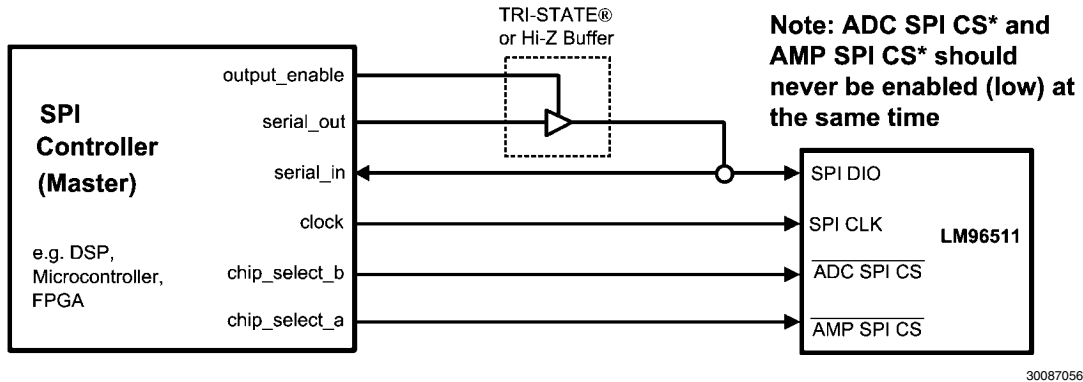


FIGURE 40. SPI™ Bus Master Slave Connection

### ACCESS TO THE SERIAL PERIPHERAL INTERFACE

The SPI™ compatible interface is accessed through the use of four pins:  $\overline{\text{ADC SPI}^\text{TM} \text{CS}}$ ,  $\overline{\text{AMP SPI}^\text{TM} \text{CS}}$ , SPI™ DIO, and SPI™ CLK. The SPI™ DIO is the data input/ output bidirectional port. The SPI™ DIO voltage levels are between the SPI™ supply voltage and ground. The SPI™ CLK acts as the SPI™ compatible clock input. Two chip selects are used to access the two functional parts of the device,  $\overline{\text{ADC SPI}^\text{TM} \text{CS}}$  for the ADC segment and  $\overline{\text{AMP SPI}^\text{TM} \text{CS}}$  for the amplifier segment. The generic timing diagram in Figure 41 shows the relative timing of the signals used to access the Serial Interface. Figure 8 and Figure 9 are included to give timing specifics for write mode and read mode respectively. Values for these specific parameters can be found in the Digital Input and Output Characteristics section of the datasheet.

The initial conditions for the SPI™ compatible signals are the beginning of an access sequence as follows: SPI™ CLK will start low, both  $\overline{\text{AMP SPI}^\text{TM} \text{CS}}$  and  $\overline{\text{ADC SPI}^\text{TM} \text{CS}}$  will start high, and SPI™ DIO will be undriven. To start an SPI™ access, either  $\overline{\text{AMP SPI}^\text{TM} \text{CS}}$  or  $\overline{\text{ADC SPI}^\text{TM} \text{CS}}$  (never both at the same time) will be brought low. At the same time, SPI™ DIO should be driven to the MSB of the address to be accessed. The SPI™ CLK will then start and rise in the center of the address bits from MSB to LSB. Each address is represented with 7 bits, A[7:1], the first 7 bits of the sequence on

SPI™ DIO. The eighth bit in the SPI™ DIO sequence, A[0] denotes a read or write access command, R/W. If the access is a read access, R/W = 1, then the user must disable the master line driven on the next falling edge of SPI™ CLK. At this point, the line will be driven by the SPI™ compatible interface of the LM96511 (slave). As the SPI™ CLK continues to toggle, the SPI™ slave will drive out the bits associated with the address input to the part D[7:0]. After the eight bits have been shifted out, the chip select can be returned high. If the access is a write access, R/W = 0, the user must drive the 8 bits associated with the address given, D[7:0], on the next eight SPI™ compatible clock cycles. After these 8 bits are shifted in, the chip select can return to the high state ending the transaction. If multiple transactions are done on a single SPI™, the associated chip select must be returned high between successive commands. During a write command, if the chip select signal is pulled high prior to the appropriate time, the write access will not be completed and the internal SPI™ compatible interface may not properly clear. At this point, a hard reset may be necessary to overcome a bad state, and writing may need to recommence. Two reset pins are also available on the LM96511, AMP RST (active HI) and  $\overline{\text{ADC RST}}$  (active LO). These reset pins will asynchronously clear the AMP SPI™ and ADC SPI™ respectively.

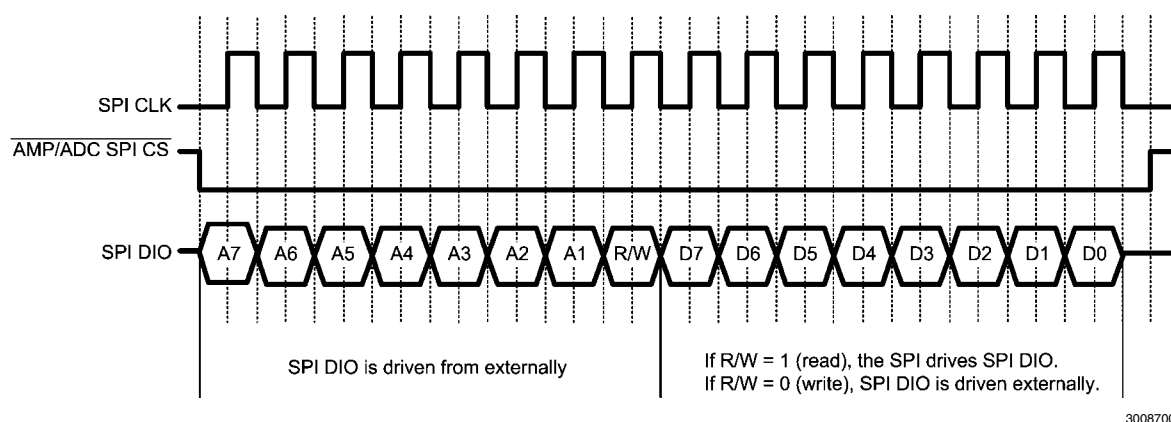


FIGURE 41. SPI™ Compatible Read/Write Timing Diagram

**CONNECTING MULTIPLE LM96511 DEVICES TOGETHER**

In certain applications, more than one LM96511 may need to be accessed by the same SPI™ compatible master controller. In this case, separate chip selects will be required for each AMP SPI™ CS pin in the system. This is due to the fact that each amplifier path will have path specific information which will need to be relayed to the paths individually. The  $\overline{\text{ADC}}$  SPI™ CS can typically be shared as the ADC channels have very few channel specific programming requirements. An ex-

ception may be made in the case of a user who would choose to power down certain ADC's in the system (done through ADC SPI™ register), in which case separate lines would be needed for each. A shared ADC SPI™ CS system is shown in Figure 42. The user must realize that connecting the chip selects of numerous chips in any system will negate the use of read mode for the affected SPI™ slaves. This is due to bus contention issues as each slave will attempt to drive its value at that address.

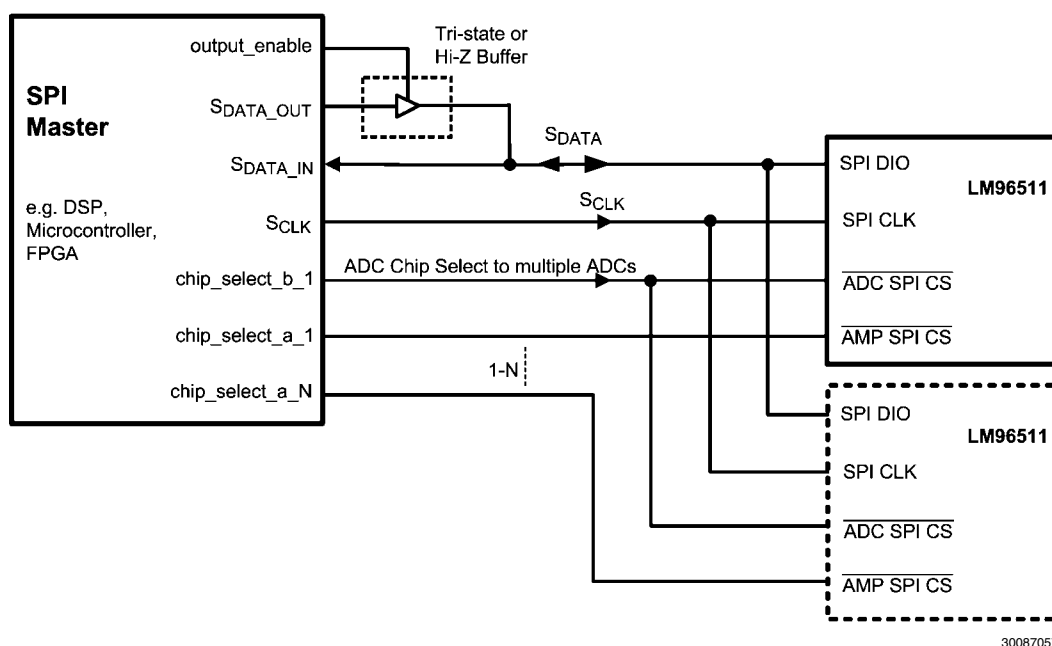


FIGURE 42. SPI™ Compatible Interconnect for Multiple LM96511's (Open Drain Mode)

**SERIAL PERIPHERAL INTERFACE READ AND WRITE SPEED**

SPI™ CLK controls the speed of interaction with the LM96511. See the Digital Input and Output Characteristics (under "SPI™") section of the datasheet for the timing information.

The following table shows the complete set of user accessible SPI™ compatible registers, with descriptions of the functionality of each bit in the following section.

## SPI™ Register Map

- The “Address” column corresponds to A7-A1 (MSB –LSB).
- A0, which is the R/W bit, is not considered as part of the address.
- “RSV” = Reserved (See notes if applicable.)

| Register Index — ADC Section (Enabled with ADC SPI™ CS): |                   |                   |                   |                    |                     |                     |                   |                   |         |
|----------------------------------------------------------|-------------------|-------------------|-------------------|--------------------|---------------------|---------------------|-------------------|-------------------|---------|
| Addr                                                     | b[7]              | b[6]              | b[5]              | b[4]               | b[3]                | b[2]                | b[1]              | b[0]              | Default |
| <b>ADC Top Control Register (Note 1)</b>                 |                   |                   |                   |                    |                     |                     |                   |                   |         |
| 00h                                                      | 0                 | 0                 | CBR               | 40/50              | SRES                | 0                   | SLEEP             | PD                | 00h     |
| <b>ADC / LVDS Channel Power Down Register (Note 2)</b>   |                   |                   |                   |                    |                     |                     |                   |                   |         |
| 01h                                                      | PD7               | PD6               | PD5               | PD4                | PD3                 | PD2                 | PD1               | PD0               | 00h     |
| <b>Modulator Overload Control Register (Note 3)</b>      |                   |                   |                   |                    |                     |                     |                   |                   |         |
| 02h                                                      | 0                 | 0                 | 0                 | IOR                | 0                   | 0                   | 0                 | 0                 | 00h     |
| <b>PLL Control Register (Note 4)</b>                     |                   |                   |                   |                    |                     |                     |                   |                   |         |
| 03h                                                      | 0                 | 0                 | 0                 | 0                  | 0                   | 0                   | SHBW              | STCAL             | 00h     |
| <b>LVDS Input Clock Hysteresis (Note 5)</b>              |                   |                   |                   |                    |                     |                     |                   |                   |         |
| 05h                                                      | 0                 | 0                 | INVCLK            | 100HYS             | 50HYS               | 20HYS               | 10HYSOFF          | HYSOFF            | 00h     |
| <b>Serializer Custom Pattern 0 Register (Note 6)</b>     |                   |                   |                   |                    |                     |                     |                   |                   |         |
| 08h                                                      | Custom Pattern[7] | Custom Pattern[6] | Custom Pattern[5] | Custom Pattern [4] | Custom Pattern [3]  | Custom Pattern [2]  | Custom Pattern[1] | Custom Pattern[0] | 00h     |
| <b>Serializer Custom Pattern 1 Register (Note 6)</b>     |                   |                   |                   |                    |                     |                     |                   |                   |         |
| 09h                                                      | 0                 | 0                 | 0                 | 0                  | Custom Pattern [11] | Custom Pattern [10] | Custom Pattern[9] | Custom Pattern[8] | 00h     |
| <b>Decimator Clipping Control Register (Note 7)</b>      |                   |                   |                   |                    |                     |                     |                   |                   |         |
|                                                          |                   |                   |                   | DGFa               |                     | DGFb                |                   |                   |         |
| 0Ah                                                      | CGS               | 0                 | a[2]              | a[1]               | a[0]                | b[2]                | b[1]              | b[0]              | 00h     |
| <b>Decimator Control Register (Note 8)</b>               |                   |                   |                   |                    |                     |                     |                   |                   |         |
| 0Bh                                                      | 0                 | 0                 | 0                 | EQON               | DFS                 | MSB                 | TSEL[1]           | TSEL[0]           | 00h     |
| <b>LVDS Control Register (Note 9)</b>                    |                   |                   |                   |                    |                     |                     |                   |                   |         |
| 0Ch                                                      |                   | 0                 | 0                 | TX_term            | I_drive [1]         | I_drive[0]          | OCM               | SLVS              | 00h     |
| <b>ADC Die ID (Read Only)</b>                            |                   |                   |                   |                    |                     |                     |                   |                   |         |
| 0Fh                                                      |                   | RSV               | RSV               | RSV                | RSV                 | RSV                 | RSV               | RSV               | N/A     |

| Register Index— Amplifier Section (Enabled with AMP SPI™ CS): |   |   |   |   |           |           |           |           |     |
|---------------------------------------------------------------|---|---|---|---|-----------|-----------|-----------|-----------|-----|
| <b>Doppler Controls (Note 10)</b>                             |   |   |   |   |           |           |           |           |     |
| 11h                                                           | 0 | 0 | 0 | 0 | CH0 PH[3] | CH0 PH[2] | CH0 PH[1] | CH0 PH[0] | 00h |
| 12h                                                           | 0 | 0 | 0 | 0 | CH1 PH[3] | CH1 PH[2] | CH1 PH[1] | CH1 PH[0] | 00h |
| 13h                                                           | 0 | 0 | 0 | 0 | CH2 PH[3] | CH2 PH[2] | CH2 PH[1] | CH2 PH[0] | 00h |
| 14h                                                           | 0 | 0 | 0 | 0 | CH3 PH[3] | CH3 PH[2] | CH3 PH[1] | CH3 PH[0] | 00h |
| 15h                                                           | 0 | 0 | 0 | 0 | CH4 PH[3] | CH4 PH[2] | CH4 PH[1] | CH4 PH[0] | 00h |
| 16h                                                           | 0 | 0 | 0 | 0 | CH5 PH[3] | CH5 PH[2] | CH5 PH[1] | CH5 PH[0] | 00h |
| 17h                                                           | 0 | 0 | 0 | 0 | CH6 PH[3] | CH6 PH[2] | CH6 PH[1] | CH6 PH[0] | 00h |

| Register Index— Amplifier Section (Enabled with AMP SPI™ CS):        |                     |                     |               |                    |                                                       |               |               |                     |             |
|----------------------------------------------------------------------|---------------------|---------------------|---------------|--------------------|-------------------------------------------------------|---------------|---------------|---------------------|-------------|
| 18h                                                                  | 0                   | 0                   | 0             | 0                  | CH7<br>PH[3]                                          | CH7<br>PH[2]  | CH7<br>PH[1]  | CH7<br>PH[0]        | 00h         |
| <b>Individual CW Doppler Channel Phase Update Register (Note 11)</b> |                     |                     |               |                    |                                                       |               |               |                     |             |
| 19h                                                                  | CS7                 | CS6                 | CS5           | CS4                | CS3                                                   | CS2           | CS1           | CS0                 | 00h         |
| <b>DVGA Attenuation Control Register (Note 12)</b>                   |                     |                     |               |                    |                                                       |               |               |                     |             |
| 1Ah                                                                  | 0                   | 0                   | 0             | 0                  | Half<br>Step<br>Disable<br>(0=0.05<br>db;<br>1=0.1db) | R_EN          | R1            | R0                  | 00h         |
| <b>LNA Offset Trim (Note 13)</b>                                     |                     |                     |               |                    |                                                       |               |               |                     |             |
| 1Bh                                                                  | LNA Ch0<br>Polarity | LNA Ch0<br>D6 (MSB) | LNA Ch0<br>D5 | LNA Ch0<br>D4      | LNA Ch0<br>D3                                         | LNA Ch0<br>D2 | LNA Ch0<br>D1 | LNA Ch0<br>D0 (LSB) | Factory Set |
| 1Ch                                                                  | LNA Ch1<br>Polarity | LNA Ch1<br>D6 (MSB) | LNA Ch1<br>D5 | LNA Ch1<br>D4      | LNA Ch1<br>D3                                         | LNA Ch1<br>D2 | LNA Ch1<br>D1 | LNA Ch1<br>D0 (LSB) | Factory Set |
| 1Dh                                                                  | LNA Ch2<br>Polarity | LNA Ch2<br>D6 (MSB) | LNA Ch2<br>D5 | LNA Ch2<br>D4      | LNA Ch2<br>D3                                         | LNA Ch2<br>D2 | LNA Ch2<br>D1 | LNA Ch2<br>D0 (LSB) | Factory Set |
| 1Eh                                                                  | LNA Ch3<br>Polarity | LNA Ch3<br>D6 (MSB) | LNA Ch3<br>D5 | LNA Ch3<br>D4      | LNA Ch3<br>D3                                         | LNA Ch3<br>D2 | LNA Ch3<br>D1 | LNA Ch3<br>D0 (LSB) | Factory Set |
| 1Fh                                                                  | LNA Ch4<br>Polarity | LNA Ch4<br>D6 (MSB) | LNA Ch4<br>D5 | LNA Ch4<br>D4      | LNA Ch4<br>D3                                         | LNA Ch4<br>D2 | LNA Ch4<br>D1 | LNA Ch4<br>D0 (LSB) | Factory Set |
| 20h                                                                  | LNA Ch5<br>Polarity | LNA Ch5<br>D6 (MSB) | LNA Ch5<br>D5 | LNA Ch5<br>D4      | LNA Ch5<br>D3                                         | LNA Ch5<br>D2 | LNA Ch5<br>D1 | LNA Ch5<br>D0 (LSB) | Factory Set |
| 21h                                                                  | LNA Ch6<br>Polarity | LNA Ch6<br>D6 (MSB) | LNA Ch6<br>D5 | LNA Ch6<br>D4      | LNA Ch6<br>D3                                         | LNA Ch6<br>D2 | LNA Ch6<br>D1 | LNA Ch6<br>D0 (LSB) | Factory Set |
| 22h                                                                  | LNA Ch7<br>Polarity | LNA Ch7<br>D6 (MSB) | LNA Ch7<br>D5 | LNA Ch7<br>D4      | LNA Ch7<br>D3                                         | LNA Ch7<br>D2 | LNA Ch7<br>D1 | LNA Ch7<br>D0 (LSB) | Factory Set |
| <b>Post Amp (PA) Offset Trim (Note 13)</b>                           |                     |                     |               |                    |                                                       |               |               |                     |             |
| 23h                                                                  | 0                   | 0                   | 0             | PA Ch0<br>Polarity | PA Ch0<br>D3<br>(MSB)                                 | PA Ch0<br>D2  | PA Ch0<br>D1  | PA Ch0 D3<br>(LSB)  | Factory Set |
| 24h                                                                  | 0                   | 0                   | 0             | PA Ch1<br>Polarity | PA Ch1<br>D3<br>(MSB)                                 | PA Ch1<br>D2  | PA Ch1<br>D1  | PA Ch1 D3<br>(LSB)  | Factory Set |
| 25h                                                                  | 0                   | 0                   | 0             | PA Ch2<br>Polarity | PA Ch2<br>D3<br>(MSB)                                 | PA Ch2<br>D2  | PA Ch2<br>D1  | PA Ch2 D3<br>(LSB)  | Factory Set |
| 26h                                                                  | 0                   | 0                   | 0             | PA Ch3<br>Polarity | PA Ch3<br>D3<br>(MSB)                                 | PA Ch3<br>D2  | PA Ch3<br>D1  | PA Ch3 D3<br>(LSB)  | Factory Set |
| 27h                                                                  | 0                   | 0                   | 0             | PA Ch4<br>Polarity | PA Ch4<br>D3<br>(MSB)                                 | PA Ch4<br>D2  | PA Ch4<br>D1  | PA Ch4 D3<br>(LSB)  | Factory Set |
| 28h                                                                  | 0                   | 0                   | 0             | PA Ch5<br>Polarity | PA Ch5<br>D3<br>(MSB)                                 | PA Ch5<br>D2  | PA Ch5<br>D1  | PA Ch5 D3<br>(LSB)  | Factory Set |
| 29h                                                                  | 0                   | 0                   | 0             | PA Ch6<br>Polarity | PA Ch6<br>D3<br>(MSB)                                 | PA Ch6<br>D2  | PA Ch6<br>D1  | PA Ch6 D3<br>(LSB)  | Factory Set |
| 2Ah                                                                  | 0                   | 0                   | 0             | PA Ch7<br>Polarity | PA Ch7<br>D3<br>(MSB)                                 | PA Ch7<br>D2  | PA Ch7<br>D1  | PA Ch7 D3<br>(LSB)  | Factory Set |
| <b>Reserved Registers (RSV)</b>                                      |                     |                     |               |                    |                                                       |               |               |                     |             |

| Register Index— Amplifier Section (Enabled with AMP SPI™ CS): |       |       |       |       |       |       |       |       |     |
|---------------------------------------------------------------|-------|-------|-------|-------|-------|-------|-------|-------|-----|
| 2Bh                                                           | RSV   | RSV   | RSV   | RSV   | RSV   | RSV   | RSV   | RSV   | N/A |
| 2Ch                                                           | RSV   | RSV   | RSV   | RSV   | RSV   | RSV   | RSV   | RSV   | N/A |
| 2Dh                                                           | RSV   | RSV   | RSV   | RSV   | RSV   | RSV   | RSV   | RSV   | N/A |
| 2Eh                                                           | RSV   | RSV   | RSV   | RSV   | RSV   | RSV   | RSV   | RSV   | N/A |
| 2Fh                                                           | RSV   | RSV   | RSV   | RSV   | RSV   | RSV   | RSV   | RSV   | N/A |
| Chip ID (Read Only)                                           |       |       |       |       |       |       |       |       |     |
| 30h                                                           | Id[7] | Id[6] | Id[5] | Id[4] | Id[3] | Id[2] | Id[1] | Id[0] | N/A |

## SPI™ Register Map Notes

### 1. ADC Top Control Register

The Top Control Register is the basic initialization and control register for the LM96511 ADC.

| Bit | Description                                                                                                                                                                                                                                                                                                                                                             |
|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | <b>Write 0</b>                                                                                                                                                                                                                                                                                                                                                          |
| 5   | <b>CBR: Control Bus Read.</b> When asserted register 00h (this register) can be read, but no other registers. When de-asserted all other registers can be read, but not register 00h.<br>0: Register 00h cannot be read using SPI™ Read. All other registers can be read back.<br>1: Register 00h can be read using SPI™ Read. All other registers cannot be read back. |
| 4   | <b>40/50:</b> Selects the ADC sample rate. This bit should be set according to the applied input clock to obtain optimal performance.<br>0: 45-50MSPS<br>1: 40-45MSPS                                                                                                                                                                                                   |
| 3   | <b>SRES: Software Reset.</b> When asserted the software reset will reset the LM96511 ADC device. SRES performs the same function as the hardware reset (ADC RST pin). The SRES is self clearing in approximately 2 μs.<br>0: Software Reset Inactive<br>1: Software Reset Active                                                                                        |
| 2   | 0                                                                                                                                                                                                                                                                                                                                                                       |
| 1   | <b>SLEEP: Sleep Mode.</b> Powers down the device with the exception of the PLL and the reference blocks. The time to wake-up from sleep mode is < 10 μs.<br>0: Sleep Mode Inactive<br>1: Sleep Mode Active                                                                                                                                                              |
| 0   | <b>PD: Power Down Mode.</b> Completely powers down the device. The power up time is approximately 20 ms.<br>0: PD Mode Inactive, device operates normally<br>1: PD Mode Active, device powered down                                                                                                                                                                     |

### 2. ADC/LVDS Channel Power Down Register

The ADC/ LVDS Channel Power Down Mode Register provides the capability to independently put each ADC channel in Power Down mode.

| Bit | Description                                                                    |
|-----|--------------------------------------------------------------------------------|
| 7   | <b>PD7: Channel 7 Power Down</b><br>0: Channel Active<br>1: Channel Power Down |
| 6   | <b>PD6: Channel 6 Power Down</b><br>0: Channel Active<br>1: Channel Power Down |
| 5   | <b>PD5: Channel 5 Power Down</b><br>0: Channel Active<br>1: Channel Power Down |
| 4   | <b>PD4: Channel 4 Power Down</b><br>0: Channel Active<br>1: Channel Power Down |

| Bit | Description                                                                    |
|-----|--------------------------------------------------------------------------------|
| 3   | <b>PD3: Channel 3 Power Down</b><br>0: Channel Active<br>1: Channel Power Down |
| 2   | <b>PD2: Channel 2 Power Down</b><br>0: Channel Active<br>1: Channel Power Down |
| 1   | <b>PD1: Channel 1 Power Down</b><br>0: Channel Active<br>1: Channel Power Down |
| 0   | <b>PD0: Channel 0 Power Down</b><br>0: Channel Active<br>1: Channel Power Down |

### 3. Modulator Overload Control Register

| Bit | Description                                                                                                                                                                                                            |
|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5 | <b>Write 0</b>                                                                                                                                                                                                         |
| 4   | <b>IOR: Enable IOR On Mode (Instant Overload Recovery)</b><br>This bit can be used to quickly enable IOR mode with the default IOR settings for DGF (see register 0Ah).<br>0: IOR Mode Disabled<br>1: IOF Mode Enabled |
| 3:0 | <b>Write 0</b>                                                                                                                                                                                                         |

### 4. PLL Control Register

| Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:2 | <b>Write 0</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |
| 4   | <b>SHBW: Set PLL to High Bandwidth.</b> The selection of the PLL bandwidth permits to set the sensitivity of the PLL to input clock jitter. Less bandwidth decreases the sensitivity to input clock jitter. The PLL Bandwidth is related to the sampling frequency, the exact values of which can be found in the electrical specifications table.<br><br>The PLL will pass any input clock jitter up to the PLL bandwidth, while jitter above the PLL bandwidth will be attenuated. Low bandwidth mode should be used for high jitter input clocks, while high bandwidth mode can be used for high-quality, low jitter input clocks.<br>0: PLL bandwidth is set to Low Bandwidth (400 kHz).<br>1: PLL bandwidth is set to High Bandwidth (1.4 MHz). |
| 0   | <b>STCAL: Start VCO calibration.</b> The calibration can be manually started in order to assure that the frequency tuning margin is maximum, for example, in case of large temperature change during operation it can be useful to restart the calibration.<br>0: The VCO calibration starts automatically if a Loss of Lock is detected.<br>1: The VCO calibration is restarted.                                                                                                                                                                                                                                                                                                                                                                    |

### 5. LVDS Input Clock - Hysteresis

Affects ADC CLK input hysteresis level.

| Bit | Description                                                                                                                                                                                                            |
|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:6 | <b>Write 0</b>                                                                                                                                                                                                         |
| 5   | <b>INVCLK: Invert Input Reference Clock.</b> This bit is used to invert the input clock.<br>0: Reference input clock not inverted.<br>1: Reference input clock inverted.                                               |
| 4   | <b>100HYS: Enable 100 mV hysteresis.</b> This bit enables 100 mV hysteresis. It should be used for a CMOS input clock only.<br>0: Normal operation (10 mV hysteresis).<br>1: 100 mV hysteresis (CMOS input clock only) |
| 3   | <b>50HYS: Enable 50 mV hysteresis.</b> This bit enables 50 mV hysteresis. It should be used for a CMOS input clock only.<br>0: Normal operation (10 mV hysteresis).<br>1: 50 mV hysteresis (CMOS input clock only)     |

| Bit | Description                                                                                                                                                                                                                                                                                                             |
|-----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 2   | <b>20HYS: Enable 50 mV hysteresis.</b> This bit enables 20 mV hysteresis. It should be used for a CMOS input clock only.<br>0: Normal operation (10 mV hysteresis).<br>1: 20 mV hysteresis (CMOS input clock only)                                                                                                      |
| 1   | <b>10HYSOFF: Disable 10 mV hysteresis.</b> 10 mV hysteresis is the default setting. This bit is used to disable 10 mV hysteresis, in the case where another hysteresis setting is desired, for example when using a CMOS input clock.<br>0: 10 mV hysteresis. (LVDS Input clock only).<br>1: 10 mV hysteresis disabled. |
| 0   | <b>HYSOFF: Disable all hysteresis settings</b> This bit is used to disable all hysteresis settings.<br>0: Normal operation (10 mV hysteresis).<br>1: All hysteresis settings disabled.                                                                                                                                  |

#### 6. Serializer Custom Pattern 0 and 1 Registers

##### Address: 08h (pattern 0):

This register in conjunction with register 09h provides storage for the custom de-skew pattern. See register 0Bh for a description of how this training sequence is used.

| Bit | Description                                                                                                                                                                                                                                          |
|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:0 | <b>Custom Pattern [7:0].</b> This pattern forms the lower byte of Custom Pattern [11:0] which is output by the serializer when the Training Sequence Select bits (bits 1:0) of the Decimator Control Register are set to select Training sequence 3. |

##### Address: 09h (pattern 1):

This register in conjunction with User Register 08h provides storage for the custom de-skew pattern. See register 0Bh for a description of how this training sequence is used.

| Bit | Description                                                                                                                                                                                                                                             |
|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:4 | <b>Write 0</b>                                                                                                                                                                                                                                          |
| 3:0 | <b>Custom Pattern [11:8].</b> This pattern forms the upper 4 bits of Custom Pattern [11:0] which is output by the serializer when the Training Sequence Select bits (bits 1:0) of the Decimator Control Register are set to select Training sequence 3. |

#### 7. Decimator Clipping Control Register

| Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | <p><b>CGS: Custom Gain Setting.</b> This bit is used to override the automatic gain settings for ADC and IOR modes. If the user wishes to write a custom digital gain coefficient using a[2:0] and b[2:0] of this register, then the CGS bit must be set.</p> <p>0: Normal operation Automatic gain settings used</p> <p>1: Custom Gain Setting Gain setting from a[2:0] and b[2:0] used</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |
| 6   | <b>Write 0</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 5:3 | <p>a[2:0]: Digital Gain Coefficient. In IOR on mode, the input range of an ADC channel is limited to 3.12 Vpp. In IOR off mode the input range is 4.20 Vpp. The output of the digital filter has to be scaled according to the selected mode (the filter data has to be mapped in to the 12bit output data), the difference between 3.12 Vpp and 4.20 Vpp is -2.6 dB, hence the digital filter gain has to be set to 2.6 dB when in IOR on mode and to 0dB when in IOR off mode (default mode). This is performed by setting a Digital Gain Factor (DGF) which is calculated using the following formula:</p> $DGF = \frac{32 + 4 \times DGFa + DGFb}{26}$ <p>The mapping of the coefficient values for a[2:0] is as follows:</p> <p>011 = Not used. Defaults to 2</p> <p>010 = 2</p> <p>001 = 1</p> <p>000 = 0</p> <p>111 = -1</p> <p>110 = -2</p> <p>101 = Not used. Defaults to -2</p> <p>100 = Not used. Defaults to -2</p> <p>The mapping of the coefficient values for b[2:0] is shown below. <a href="#">Table 3</a> shows the available Digital Gain Coefficient settings.</p> |
| 2:0 | <p>The mapping of the coefficient values for b[2:0] is as follows:</p> <p>011 = Not used. Defaults to 2</p> <p>010 = 2</p> <p>001 = 1</p> <p>000 = 0</p> <p>111 = -1</p> <p>110 = -2</p> <p>101 = Not used. Defaults to -2</p> <p>100 = Not used. Defaults to -2</p>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |

TABLE 3. DGF To Digital Gain Look-Up Table

| Coefficient a[2:0] | Coefficient b[2:0] | Digital Gain (dB) | Equivalent ADC Full Scale Input Range (Vpp) |                              |
|--------------------|--------------------|-------------------|---------------------------------------------|------------------------------|
| 010                | 010                | 4.16              | 2.60                                        |                              |
| 010                | 001                | 3.95              | 2.66                                        |                              |
| 010                | 000                | 3.74              | 2.74                                        |                              |
| 010                | 111                | 3.52              | 2.80                                        |                              |
| 010                | 110                | 3.29              | 2.88                                        |                              |
| 001                | 001                | 3.06              | 2.96                                        |                              |
| 001                | 000                | 2.82              | 3.04                                        |                              |
| 001                | 111                | 2.58              | 3.12                                        | IOR ON Mode Default Setting  |
| 001                | 110                | 2.33              | 3.22                                        |                              |
| 000                | 001                | 2.07              | 3.3                                         |                              |
| 000                | 000                | 1.80              | 3.42                                        |                              |
| 000                | 111                | 1.53              | 3.52                                        |                              |
| 000                | 110                | 1.24              | 3.64                                        |                              |
| 111                | 001                | 0.95              | 3.96                                        |                              |
| 111                | 000                | 0.64              | 3.90                                        |                              |
| 111                | 111                | 0.33              | 4.04                                        |                              |
| 111                | 110                | 0                 | 4.20                                        | IOR Off Mode Default Setting |
| 110                | 001                | -0.34             | 4.32                                        |                              |
| 110                | 000                | -0.70             | 4.56                                        |                              |
| 110                | 111                | -1.07             | 4.76                                        |                              |
| 110                | 110                | -1.45             | 4.96                                        |                              |

## 8. Decimator Control Register

| Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 |
|-----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5 | <b>Write 0</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 4   | <b>EQON: Equalizer Enable.</b> This bit is used to enable or disable the digital equalizer. The equalizer can be switched on in order to reduce the group delay of the output data, at the cost of increased power.<br>0: Equalizer Disabled<br>1: Equalizer Enabled                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |
| 3   | <b>DFS: Data Format Select.</b> Selects the format, either Offset Binary or Twos Complement of the output data.<br>0: 2s Complement<br>1: Offset Binary                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                     |
| 2   | <b>MSB:</b> Select the bit order of the LVDS output data stream.<br>0: LSB first<br>1: MSB first                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            |
| 1:0 | <b>TSEL[1:0]: Training Sequence Select.</b> These bits select the LVDS output data. The default mode of operation is where the filter output data is serialized.<br>In the remaining modes the selected training sequence is repeatedly output from the serializer this allows the receiving data capture circuitry to perform the de-skewing process.<br>One of three known words can be selected, the first two words are hard-coded in the block, the third one, the custom pattern, is written into <b>Registers 08h and 09h Serializer Custom Pattern Registers</b> .<br>Note: The outputs bit-clock and word-clock are not affected by the value of the Training Sequence Select bits.<br>00 ADC data[11:0]<br>01 Training Sequence 1: 000000111111<br>10 Training Sequence 2: 101010101010<br>11 Training Sequence 3: Custom Pattern |

## 9. LVDS Control Register

| Bit | Description                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          |
|-----|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7:5 | Write 0                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              |
| 4   | <b>TX_term</b> : Enable Internal 100Ω termination for data outputs.<br>0: Internal 100Ω termination disabled.<br>1: Internal 100Ω termination enabled.                                                                                                                                                                                                                                                                                                                                                                                                               |
| 3:2 | <b>I_drive[1:0]</b> : Controls the current drive of the data outputs.<br>00: 2.5 mA<br>01: 3.5 mA<br>10: Reserved<br>11: 5mA                                                                                                                                                                                                                                                                                                                                                                                                                                         |
| 1   | <b>OCM</b> : Output Common mode. Allows the output common mode to be shifted depending on the setting of ADC IO DVDD.<br>If bit 0 of this register, SLVS, is set to 1 then changing OCM will have no impact on the output common mode. The output common mode in SLVS mode is fixed, as described in the Electrical Specifications section of this datasheet.<br>For ADC IO DVDD = 1.2V, OCM must be set to 0.<br>For ADC IO DVDD = 1.8V, OCM must be set to 1.<br>0: Output Common Mode, V <sub>OCM</sub> = 1.0V<br>1: Output Common Mode, V <sub>OCM</sub> = 1.25V |
| 0   | <b>SLVS</b> : Select the format for output data, either LVDS or SLVS. The differences in timing and electrical specifications between the two modes can be seen in the Electrical Specifications section of the datasheet. If this bit is set to 1 (SLVS mode), OCM has no effect and the output common mode will be set for SLVS as described in the Electrical Specifications section of this datasheet. When LVDS mode is selected, the output common mode must be selected using the OCM bit of this register.<br>0: LVDS Mode<br>1: SLVS Mode                   |

## 10. Doppler Controls:

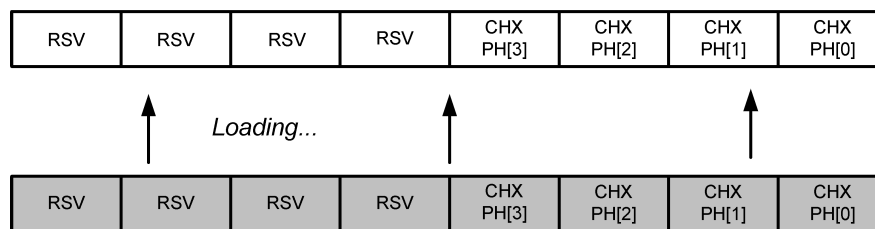
| Bit | Description                                                                                                            |
|-----|------------------------------------------------------------------------------------------------------------------------|
| 7:4 | Write 0                                                                                                                |
| 3:0 | Chx[3:0]: CW Doppler Channel “x” (0-7) phase angle in binary format from 0° (0000) to 360° (1111) in 22.5° increments. |

## 11. Individual CW Doppler Channel Phase Update

The SPI™ compatible registers for the Doppler function (i.e. 11h-18h) are shadow registers that will only be loaded into an active working register on CW CLK+ rising edge after a CW/DVGA RST (pin K15) pulse (see [Figure 10](#)). This load action will also reset all counters in the CW Doppler mixer.

Upon initial chip power-up, CW Doppler register load and mixer counter reset occurs (see SPI™ Register Map for default values). SPI™ Read operation reads the value of the Shadow register (not the Active register). However, Shadow and Active register values should be the same assuming no Write operation after the previous CW/DVGA RST high state.

Active Register



SPI Register (Shadow Register)

**Figure 41. CW Doppler Shadow Register Representation**

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In addition to being able to load all CW Doppler channels 0-7 phase angles simultaneously, it is also possible to load each channel's phase angle individually using SPI™ address 19h. For example, to update phase angle for channel 5 and channel

6 only, the following data is written to 19h: 01100000. This way, Channel 5 and 6 Active register is updated with data in 16h and 17h but Active registers for the other 6 channels are left intact.

| Bit | Description                                                                                                                                                                                                                                          |
|-----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 7   | <b>CS7:</b> This bit allows CW Doppler channel 7 phase angle to be updated to the value in shadow register 18h.<br>0: Active register for channel 7 left intact<br>1: Load active register for channel 7 with 18h data when CW/DVGA RST is pulled HI |
| 6   | <b>CS6:</b> This bit allows CW Doppler channel 6 phase angle to be updated to the value in shadow register 17h.<br>0: Active register for channel 6 left intact<br>1: Load active register for channel 6 with 17h data when CW/DVGA RST is pulled HI |
| 5   | <b>CS5:</b> This bit allows CW Doppler channel 5 phase angle to be updated to the value in shadow register 16h.<br>0: Active register for channel 5 left intact<br>1: Load active register for channel 5 with 16h data when CW/DVGA RST is pulled HI |
| 4   | <b>CS4:</b> This bit allows CW Doppler channel 4 phase angle to be updated to the value in shadow register 15h.<br>0: Active register for channel 4 left intact<br>1: Load active register for channel 4 with 15h data when CW/DVGA RST is pulled HI |
| 3   | <b>CS3:</b> This bit allows CW Doppler channel 3 phase angle to be updated to the value in shadow register 14h.<br>0: Active register for channel 3 left intact<br>1: Load active register for channel 3 with 14h data when CW/DVGA RST is pulled HI |
| 2   | <b>CS2:</b> This bit allows CW Doppler channel 2 phase angle to be updated to the value in shadow register 13h.<br>0: Active register for channel 2 left intact<br>1: Load active register for channel 2 with 13h data when CW/DVGA RST is pulled HI |
| 1   | <b>CS1:</b> This bit allows CW Doppler channel 1 phase angle to be updated to the value in shadow register 12h.<br>0: Active register for channel 1 left intact<br>1: Load active register for channel 1 with 12h data when CW/DVGA RST is pulled HI |
| 0   | <b>CS0:</b> This bit allows CW Doppler channel 0 phase angle to be updated to the value in shadow register 11h.<br>0: Active register for channel 0 left intact<br>1: Load active register for channel 0 with 11h data when CW/DVGA RST is pulled HI |

#### 12. DVGA Attenuation Control:

When the CW/DVGA RST pin is HIGH, the step attenuator block in the DVGA can be reset to one of five discrete selectable DVGA Initial Attenuations: 38, 36, 34, 32, or 0 dB. This DVGA Initial Attenuation can be set by either the SPI™ compatible register or by physically applying logic level voltages to ball pin A6 (DVGA INIT MSB), B5 (DVGA INIT LSB), and L17 (DVGA UP). See [Table 4](#). SPI™ address 1Ah[2:0] are the register bits used. Normal attenuator gain clocking can be resumed only after CW/DVGA RST pin is returned to 0.

**TABLE 4. DVGA Initial Attenuation Truth Table**

| DVGA UP | E_EN   | R1     | R0     | DVGA INIT MSB | DVGA INIT LSB | Attenuation with CW/DVGA RST pin High (dB) |
|---------|--------|--------|--------|---------------|---------------|--------------------------------------------|
| L17 pin | 1Ah[2] | 1Ah[1] | 1Ah[0] | A6 pin        | B5 pin        |                                            |
| 1       | 1      | 0      | 0      | X             | X             | 38                                         |
| 1       | 1      | 0      | 1      | X             | X             | 36                                         |
| 1       | 1      | 1      | 0      | X             | X             | 34                                         |
| 1       | 1      | 1      | 1      | X             | X             | 32                                         |
| 1       | 0      | X      | X      | 0             | 0             | 38                                         |
| 1       | 0      | X      | X      | 0             | 1             | 36                                         |
| 1       | 0      | X      | X      | 1             | 0             | 34                                         |
| 1       | 0      | X      | X      | 1             | 1             | 32                                         |
| 0       | X      | X      | X      | X             | X             | 0                                          |

The following short-hand notation for the DVGA gain has been used:

TABLE 5. DVGA Notation

| DVGA Gain (dB) | DVGA Attenuation (dB) | Short-hand Name |
|----------------|-----------------------|-----------------|
| 0              | 0                     | Max DVGA Gain   |
| -19            | 19                    | Mid DVGA Gain   |
| -38            | 38                    | Min DVGA Gain   |

13. **LNA and PA Offset Trim Control Register:**

There are 7 bits dedicated to LNA offset trim, plus the polarity bit. The maximum positive offset is 1111,1111 and the maximum negative offset is 0111,1111 with X000,0000 for minimum trim.

There are 4 bits dedicated to PA offset trim, plus the polarity bit. The maximum positive offset is 1,1111 and the maximum negative offset is 0,1111 with X,0000 for minimum trim.

The SPI™ compatible trim data operates through the same die fuses that are used for factory laser trim. The data written into a particular bit is influenced by whether the fuse related to that bit is blown at the factory or not. Here is what should be written to the SPI™ compatible bits for a particular “intended data”:

TABLE 6. Offset Trim “Write” Truth Table

| Intended Data | Write Data         |                       |
|---------------|--------------------|-----------------------|
|               | Factory Blown Fuse | Factory Un-Blown Fuse |
| 0             | 1                  | 0                     |
| 1             | 0                  | 1                     |

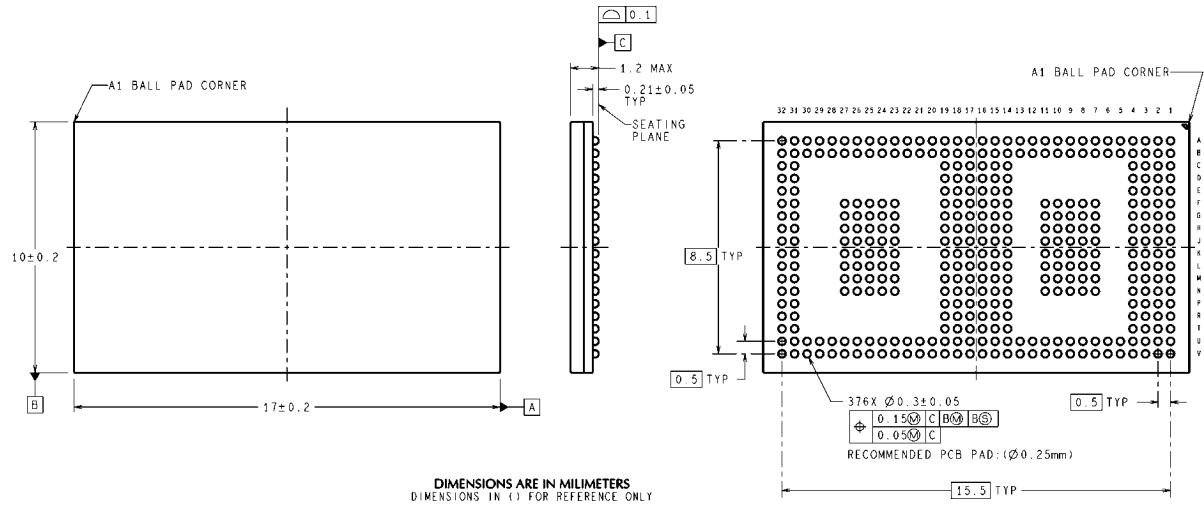
To know whether a fuse is blown at the factory or not, the register should be read-back at power up (or after AMP RST pulse); a “1” indicates a blown fuse.

Here is an example, related to LNA offset trim, for easier understanding:

TABLE 7. Offset Trim “Write” and “Read” Example

|                                             |           |
|---------------------------------------------|-----------|
| SPI™ Read Back at Power-up or after AMP RST | 0000 1100 |
| <i>Intended Data</i>                        | 0000 1010 |
| SPI™ Write Data                             | 0000 0110 |
| SPI™ Read Data (after Write)                | 0000 1010 |

# Physical Dimensions inches (millimeters) unless otherwise noted



TBD

SLM376A (Rev A)



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| Interface                      | <a href="http://www.national.com/interface">www.national.com/interface</a>     | Eval Boards                  | <a href="http://www.national.com/evalboards">www.national.com/evalboards</a>       |
| LVDS                           | <a href="http://www.national.com/lvds">www.national.com/lvds</a>               | Packaging                    | <a href="http://www.national.com/packaging">www.national.com/packaging</a>         |
| Power Management               | <a href="http://www.national.com/power">www.national.com/power</a>             | Green Compliance             | <a href="http://www.national.com/quality/green">www.national.com/quality/green</a> |
| Switching Regulators           | <a href="http://www.national.com/switchers">www.national.com/switchers</a>     | Distributors                 | <a href="http://www.national.com/contacts">www.national.com/contacts</a>           |
| LDOs                           | <a href="http://www.national.com/ldo">www.national.com/ldo</a>                 | Quality and Reliability      | <a href="http://www.national.com/quality">www.national.com/quality</a>             |
| LED Lighting                   | <a href="http://www.national.com/led">www.national.com/led</a>                 | Feedback/Support             | <a href="http://www.national.com/feedback">www.national.com/feedback</a>           |
| Voltage References             | <a href="http://www.national.com/vref">www.national.com/vref</a>               | Design Made Easy             | <a href="http://www.national.com/easy">www.national.com/easy</a>                   |
| PowerWise® Solutions           | <a href="http://www.national.com/powerwise">www.national.com/powerwise</a>     | Applications & Markets       | <a href="http://www.national.com/solutions">www.national.com/solutions</a>         |
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